A REAL-TIME DATA ACQUISITION SYSTEM FOR THE MEDIUM SCALE INDUSTRIAL PLANT IN KENYA: A CASE STUDY AND SOLUTION AT CMB PACKAGING LTD., THIKA.

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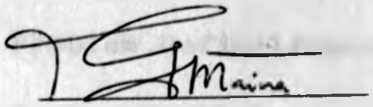
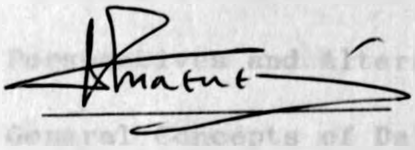
This thesis is my original work and has not been presented for a degree in any other University.



Peter G. Maina

This thesis has been submitted with my approval as University supervisor.



Dr. S.H. Mneney

Contents

List of Abbreviations.

a.c	alternating current
AWGN	Additive White Gaussian Noise
A/D	Analogue to Digital
ASCII	American Standard Code for Information Interchange
BW	Bandwidth
CAM	Computer Aided Manufacturing
CIM	Computer Integrated Manufacturing
CJC	cold junction compensation
CL	Current Loop
CMB	CMB Packaging Ltd., Thika.
CMOS	Complementary Metal Oxide Semiconductor
CNR	carrier-to-noise power ratio
D.A.S.	Data Acquisition System
d.c.	direct current
DPSK	Differentially coherent Phase Shift Keying
ECL	Emitter Coupled Logic
EEPROM	Electrically Eraseable Programmable Read Only Memory
EMI	Electromagnetic Interference
F.I.S.	Factory Information Systems
FM	Frequency Modulation

IC	integrated circuit
I/O	input/output
pcb	printed circuit board
PLC	Programmable Logic Controller
PSD	power spectral density
PSK	Phase Shift Keying
RAM	Random Access Memory
r.m.s.	root mean square
ROM	Read Only Memory
RTD	resistance temperature device
SE	shielding effectiveness
SNR	signal-to-noise ratio
TC	thermocouple
TT	Transducer-Transmitter
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receiver Transmitter
U.D.T.	User-end Data Terminal

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ABSTRACT

Collection of manufacturing information (data acquisition) is motivated in varying degrees by the needs to make informed decisions on an urgent basis on the shop floor, analyse factors for strategic planning or archive useful facts for historical reference. In each case good decisions are a direct result of accurate, up to date and easily retrievable information. In the manufacturing situation such information often changes unpredictably; shifts, raw material, processing parameters and product quality all arise in various combinations. Even the medium sized manufacturing plant generates a daunting mass of action-demanding information whose interpretation in good time may be critical to a firm's profitability. Thus collection of operational data as it occurs (in real time) is a first critical step in optimizing production. The next steps include the organisation of the data and its informative presentation to the human or automated decision-maker. The data acquisition

problem starts with the capture of the raw manufacturing process information and ends with its application by a user.

In this Thesis the problem of collecting and interpreting production and process information in medium to large scale manufacturing plants is exposed and briefly discussed. It is shown why automating the data handling in such cases is usually the most viable solution. The tinplate printing department at CMB Packaging Ltd. "open-top" factory at Thika is given as a typical example. It is further explained how the existing information capture and archiving system is becoming rapidly obsolete and must be replaced. In this context it is shown why commercially available replacement systems are unsatisfactory on technical and cost grounds.

The Thesis documents the information (data) acquisition problem in the Printing Department and analyses and specifies the characteristics of the efficient replacement system. It then proposes a general approach to the electronic hardware required in the solution of similar data acquisition problems. These may be in industry, water treatment or any other

operations where widely distributed remote activities require simultaneous monitoring and thus making electronic telemetering a worthwhile consideration. In this work a microprocessor based data acquisition system has been specified, designed and implemented. Although specifically efficient for the Printing Department at CMB Packaging, the design is meant to be easily adaptable to other production centres either in the factory itself or elsewhere. The system is designed to operate autonomously (without frequent operator intervention) but compatibility is retained for uses where the system may be required to interact with a general-purpose computer. Measured performance of this prototype shows excellent correlation with design requirements. Cost estimates on the system indicate an advantage in its favour exceeding 2:1 over comparable commercially marketed systems. It is expected that this work convincingly demonstrates a practical approach to the data acquisition problem in general and a viably cost-effective hardware solution in particular. With little extra development the prototype should be found an immensely more attractive alternative to commmercially available

systems for the data acquisition needs of the medium scale factory in Kenya.

The Thesis itself is divided into three distinct Parts. Part I covers background material including the problem definition, scope of work and a brief summary of the significant results of this work. It also contains most other introductory material related to the project. Part II covers the theoretical aspects of the project and includes most of the material required for design purposes of the Data Acquisition System (D.A.S.). It is intended to serve secondarily as an illustrative procedure if a design is needed that is distinctly different from the one presented here. Part III describes how the prototype system proposed for the CMB Thika situation was realised. It therefore concentrates on the specific practical details of this project.

The concept of this project was based on the hope that it will be of direct and immediate relevance to an instrumentation engineer in industry. In this regard, it is intended that the presentational style of this Thesis be direct and compact enough to be of practical use to the field engineer. Thus a deliberate

attempt is made to shorten descriptive text and improve clarity by using text to supplement rather than repeat information on diagrams. Similarly, lengthy mathematical derivations are left out in favour of appropriate reference texts. It is hoped that these make it a more useful document for the engineer wishing to adapt or develop the prototype or apply the results and methods to his own situation.

While the modular approach taken in the design for this project enables the results to be applied to a wide variation of factory sizes we use the term *medium scale* to imply a factory employing an order of *tens* of transducers. Specifically the case study considers the monitoring of 50 independent information sources of bandwidth not exceeding 10 Hz each.

PART I

Background

This Part lays the foundations required to put the idustrial data acquisition problem in proper context. It covers in general terms the scope of this problem and states briefly the significant results of this project.

CHAPTER 1

INTRODUCTION

In manufacturing, it may be said that every action will ultimately trickle down to a company's Profit-and-Loss Account. Thus every decision maker needs to be supported by as much information as possible. Decision makers include those who make policy, those who plan and oversee implementation and the ones who actually execute the policies. In this project we investigated a way of obtaining and presenting production process information to the first line decision makers; the line operator, the production engineer and the production manager. We were particularly concerned with gathering and transmitting this information in the cheapest way possible. The reason for this is that often the medium scale company in Kenya finds itself in a difficult situation with regard to modernisation. On one hand it finds that it has reached a point in its growth where it can only expand further if it invests in more advanced production technology, processes and methods.

On the other hand it finds itself unable to raise all the requisite funds. In this Thesis a low cost solution, apparently the only option is proposed.

The approaches to the solution of this problem can basically be categorised in terms of the level of sophistication and the extent of the automation employed. At one extreme is Computer Integrated Manufacturing (C I M) whereby the whole manufacturing process is unified, automated and coordinated through a computer network. This includes such traditionally non-production functions as Sales, Accounting and Personnel. The benefits of this approach in relation to its considerable complexity and capital cost remain controversial as a generalised remedy [1]. On the other extreme is manual logging of data on standardised sheets. While historically this was predominant because of being apparently cheap, this is no longer clearly so. Labour costs have soared and increased sophistication in manufacturing has raised timing and accuracy demands to levels often unachievable manually. Even in slow processes manual data gathering is not without deficiency or weakness. All operator intervention in the taking of production

figures, process data and alarm reporting is open to abuse, error, neglect and incompetence. Downtime can be misreported, data charts lost, instrument settings erroneously done and clear system alarms ignored. In the above and many other instances, confusion, damage to product and lack of certainty as to blame placement often arise. While not all of these problems can be solved with a good automated data collection system, it will go a long way in alleviating many of them. Thus industrial data acquisition has progressively evolved towards more automation [1].

As will often happen, while the company may have a cash availability problem, skilled manpower may be easily available. That is, it is possible that the cost of the skilled labour required to develop a piece of equipment in-house is lower than the cost of a purchase. In this case it makes good business sense to invest in an in-house technology development programme. Companies in this kind of situation would benefit most from the approach we have taken in this project. From personal experience CMB Packaging Ltd., Thika was identified as one such company and thus used as a case study. Our primary concern was necessarily

the technology problem rather than information management. As such this project deals only with *data acquisition, transmission and recovery* and dwells little on data presentation.

The particular case of CMB Packaging Ltd., Thika, presents an interesting study of industrial data acquisition. The factory was established long before electronics made large scale automation possible. But new business realities have led to the adoption of a rapid modernisation programme at the site. The result is that production technologies seperated by nearly half a century in time are in use side by side, giving a good comparative assessment. Further, the modernisation work has raised at all operational levels the vital questions: is it necessary to change? If so where? Is it economically feasible? Change to what? Should change be piecemeal or complete overhaul? How much will the least beneficial change cost? *etc.* The motivation for doing the work in this Thesis arose from the notion that many factories have to face very similar questions at some time in their lifecycle. In this case rarely are there simple answers to these questions. In this research we narrow down to the

problem of the modernisation of production technology where we isolate the issue of instrumentation. Our objective here is to delineate the critical factors and quantify them as far as possible and thus hopefully lead to a systematic way of approaching them.

While acknowledging that factory modernisation touches a very broad spectrum of activities such as premises infrastructure, personnel *etc.*, our main interest is drawn to the production technology itself. Here we differentiate between production machinery and the instrumentation that enables operators to control and monitor production. It is the instrumentation problem that this Thesis addresses because it is where the most flexible scope of solution strategies is available in an already established factory. (Production machinery is already type-specified by the desired final product). We further split instrumentation into monitoring-oriented and control-oriented functions. The raw material for each of the operations is process data which in an industrial context must be captured in real time from different variables at distributed sources. The end of

either operation is when the captured data is used by a monitoring or control device to reach some decision. We treat this device as the end user of the captured data. Thus the scope of the problem that we deal with in this Thesis covers the sensing of data from different variables at distributed sources, its transmission in operational conditions and reception and recovery by a centralised remote end user. At the reception point the data is formatted for access by a real-time monitor, analyser or archiving device external (peripheral) to the proposed system. Such a device may be a computer, tape recorder or printer. Work done was limited to the point where the acquired data is accessible to such devices via a standard interface.

In seeking to deal with the question of collecting manufacturing information, a large number of approaches and choices exist. In many cases technical personnel facing this problem will try to appreciate the general situation and then search out sales catalogues for equipment that may be appropriate. Consequently equipment is selected on vague criteria without critical appraisal of its capabilities. In

other instances special needs may arise for which no ready equipment is being marketed or in which the equipment is so expensive as to be unaffordable. The view in this Thesis is that the data acquisition problem in all of these contexts can and should be explicitly defined and quantified. That by breaking down this problem in precise form an efficient data gathering system can be specified. And that from this specification the most cost-effective solution can be arrived at either through purchase or customized design. Thus a general methodology is illustrated in this Thesis for addressing the data acquisition problem. The progression from this to a design solution for a specific case study is shown and proven by execution in hardware. CMB Packaging Ltd., Thika provided the case study. Apart from the disparities in the level of technology in use as already mentioned, it provided challenging problems in terms of the physical environment and variety of information sources. The rapid changes going on in its production systems also required a forward-looking solution that can meet the drastically different needs of tomorrow.

While a generalised approach to the data

acquisition problem in the industrial context is highly desirable, the final solution takes advantage of opportunities offered by the specific problem at the CMB Packaging Ltd. site. As a result, while the analysis of the problem is quite general a certain loss of this generality may be expected in the practical solution stages. The problem analysis is expected to be widely applicable to situations such as in industry, water treatment *etc.* where remotely distributed activities require simultaneous monitoring. The proposed practical solution is considered generally appropriate for all operations at CMB but is specifically optimised for its Printing Department. A hardware prototype system was designed, built and tested on this premise.

The prototype (referred to here as the Data Acquisition System (D.A.S.)) is intended to operate autonomously initially in parallel with the existing systems. It was tested under simulated Printing Dept. conditions in the laboratories both at the University of Nairobi and CMB. While actual operational trials on site were not possible, test results showed very good correlation between design expectations and

actual performance. It was possible to show that variable sensing, information transmission and recovery were feasible as proposed. It was demonstrated that the proposed D.A.S. is more attractive to the Kenyan factory on grounds of cost/performance than commercially competing units. A cost advantage in excess of 2:1 in favour of the D.A.S. can be realistically anticipated. The key limiting factors in the implementation of the proposal by target factory were identified. These narrow down to the unavailability of a microprocessor development system and weak electronic prototyping support facilities locally. Simple solutions to nearly all the problem areas encountered in this work can be found if such facilities become available. For example, it would enable more extensive real-time software development for the D.A.S. as it is not exhaustively dealt with here. Such facilities would also enable meaningful extension of related research as pointed out in the Thesis. With this in mind we now proceed to a more formal statement of the problem.

1.1 Problem definition.

a. The problems.

This research project set out to tackle two major problems. First to formulate a general approach to the design of a manufacturing information gathering system for industry. This information includes process variables such as temperature, pressure, level and flow rates. It also includes material data such as item counting, machine speeds and alarm triggers. Thus the development of a general methodology is desired for dealing with data acquisition problems in different situations.

Secondly, we sought to demonstrate a prototype design following the approach suggested. Consequently it appeared reasonable that a case-study approach would be best. It was then possible to illustrate how the general methodology can be applied to a specific situation. (CMB Packaging was chosen due to its previous familiarity to the author). It needs to be stated however that by going into detail in illustrating the methods and concepts it is not intended that one need move on to a design. Rather a case study approach is used to demonstrate how the

general methodology can be translated into a specific solution. In fact all the work done for Parts I and II of this research was intended to be as useful to a factory engineer wishing to purchase a data acquisition unit as one preferring to design the complete system. This raises the question; if data acquisition units are commercially available, why build one? The reasons in this case are given below.

b. The Solution.

There were two main reasons why this was done. One is that what is commercially available are essentially data acquisition units and not systems. This needs further qualification. Take the prototype system in this Thesis. It was designed for at least 48 channels and to cover at least 15000 m^2 of shop floor space. It is modular (physically easily re-configurable) and easily adaptable and expandable to meet changing needs. On the other hand a comparable commercial unit is a single entity designed to perform well for widely varying customers. It is designed on the assumption that it will reside at a minimal distance from the monitored process. Thus if a particular situation

calls for information to be transmitted for fairly long distances (100 m and over) special arrangements and possibly new equipment and design costs must be applied. In this way the single unit now expands into a system.

The second consideration in deciding to build rather than buy a D.A.S. is cost. For wide commercial appeal, a commercial unit must include wide performance levels. Thus in most instances there will be superfluous features for a specific customer. Effectively the customer then pays for features he does not need. In this case a user needs to investigate whether his own purpose-built system would be cheaper. For the CMB case it was found that it will be immensely cheaper to design the system. To illustrate this, a commercially available unit of comparable specification [2], excluding interfacing and network design costs would have cost in excess of KSh. 80,000 ex-factory U.S.A. On the other hand, the prototype cost approximately KSh. 35,000 and although more expenditure must be made before a production version is available, the cost advantage is clear. The issue is not just cost/performance ratios but also

that few factories in Kenya would be comfortable committing the size of financial outlay demanded to purchase a commercial system to this end. This may be inspite of the fact that genuine needs exist. Thus any progress towards making such a system cheaply available would in itself be useful. It was therefore decided to define the research project to consist of a study to draw up a system specification and a realization of a prototype. This is the work documented in the following pages; the attempt whose approach and most significant results are now summarised below.

1.2 Scope of Work.

The preliminary work involved consultations with factory Management, Projects Engineers and Line Operators. It was considered essential that an overall picture be available on their expectations of the role of manufacturing information gathering in general and process information in particular. This is discussed more fully in Section 2.1. The preliminary discussions led to a more detailed study and analysis in order to

draw up the technical specifications of the D.A.S. With these in mind, a systematic attempt was made to use it to lead to a generalised solution of the data acquisition problem. Then specific facts and constraints were applied to the general system so that a design appropriate for the CMB site was obtained.

The hardware and software realization of the prototype were not intended to be unique. The underlying criteria were acceptable performance at low cost. Ease of construction, trouble-shooting, maintenance and flexibility in use were the other important considerations. Thus for example the Concentrator Unit uses cheaper locally available IC's for analogue to digital conversion while a single but much more expensive IC may appear more elegant. It also uses two printed circuit boards to improve modularity while a single board would lower production cost. These practical compromises are related to specific situations and no attempt was made here to standardize them.

Finally the commissioning of the complete system

was done and its performance observed. These are also documented here and special difficulties, limitations and comments on areas for further work discussed.

1.3 Summary of Significant Results.

The evaluation was based on laboratory simulation of signal conditions expected at the CMB site.

Designs were proposed and found to perform to specification for the analogue and pulse transducer conditioner units. In particular, it was demonstrated that temperature and counting information could be successfully transmitted over a linearly modulated current in a loop scheme. A switching scheme to multiplex 48 analogue channels onto a single line was also shown to be successful. Further the circuitry proposed for performance of analogue-to-digital conversion and parallel to serial digital data transmission was demonstrated by the prototype Concentrator Unit.

It was shown that using a simple sliding window, the embedded Z80 microprocessor in the User-end Data Terminal (U.D.T.) was able to frame and synchronise arriving serial data at the system receiver unit.

Consequently the hardware implementation can be considered conclusively verified.

Although the software developement was not initially planned as a major part of the research task, an effort was made to install some simple illustrative programs in the system. This concentrated on the setting up of a basic operating system around which user-designed software could be built later. However, several application programs were also installed to illustrate both the hardware-software interfacing technique and the system output process. These software performance goals were achieved with a reasonable degree of success despite equipment limitations. This is discussed in detail in Chapter 8.

An estimate of the total cost of the project showed that on this basis the proposed approach has a decisive advantage over other commercially marketed systems.

To conclude this part on background information, Chapter 2 addresses in some detail the data acquisition problem in general and the CMB case in particular.

CHAPTER 2

DATA ACQUISITION IN THE MANUFACTURING PROCESS

Strictly speaking although the following discussion will be specific to the manufacturing situation, it applies broadly to many other areas where automated data acquisition is desirable. Such areas include water and sewerage treatment and the (chemical) process industry. The important features in the D.A.S. are: linear current transmission at the front end, digital transmission over a telemetry link and computer compatible system output. It is also noteworthy that data processing is available in the U.D.T. and may be used to the extent dictated by user needs. In the following sections we elaborate on the general concepts applied in the data collection approach for this project and specific details concerning the CMB site.

2.1 Perspectives and Alternatives.

It is important that an overall perspective be obtained of factory information systems (F.I.S.) in

general and the D.A.S. in particular. That the current trend in commerce and industry is to use more and more information technology is well known. Information technology requires a high capital input and careful attention is needed in its purchase and utilisation. Manufacturing concerns are usually faced with several options in the introduction of new information technology:

(i) Introduce new equipment in isolated operating areas strictly as the need impels.

(ii) Select large portions of the operational branches and introduce integrated (comprehensive) solutions.

(iii) Draw up an Information Systems blueprint for the whole concern and a strategy for its implementation.

While the first option is common, it is rarely found to be the most effective long term strategy. The latter two options overlap with what have come to be known as computer aided and computer integrated manufacturing (CAM/CIM). At a wider level, it is now generally accepted [1] that manufacturing concerns must begin to re-evaluate the role of the computer in

their operations. It is in this light that the impact of an automated data acquisition system in a factory must be viewed.

In particular, although we were here primarily concerned with the question of system specification, feasibility and implementation, one should not overlook how this ties up with the overall F.I.S. goals. Conceptually the proposed Printing Department D.A.S. is expected to be compatible with similar systems in all the other manufacturing operations. The underlying philosophy for its architecture not only includes re-configurability but also a capacity to be part of a factory-wide network. Consequently hardware compatibility with computer based modules was desirable at the output end as well as the flexibility of software control. The latter implies that the D.A.S. output station, the U.D.T. is not *hard-designed* to perform only one task. Rather, that is determined by the software in place. For example, it could be configured to operate as the receiver/output interface of the stand-alone D.A.S. Or else as one station of a network of similar D.A.S.'s. Or even as a satellite station of a computer supervised

factory-wide system. For this reason, the U.D.T. uses a microprocessor embedded for dedicated D.A.S. service. Most of the essential hardware is in place for the use of the U.D.T. as a special purpose microcomputer. Expansion capacity is availed to allow a user to customize it for specific needs. Thus decisions as to its ultimate configuration are the domain of the user.

For the situation at CMB it is expected that the D.A.S. will in future be linked up with the current project to transfer line control to programmable logic controllers (PLC's). Whether the requisite D.A.S. as analysed in these following pages is actually purchased in parts or in whole or developed *in-house* at CMB remains a Management decision. What is of specific interest now at this point is the question of the feasibility of developing such a system in-house . Of particular interest apart from technical performance are capital and running costs, availability of spares and suitability to specific factory needs. It is attempted to illustrate by example in Part III that such a system can be developed at particularly low cost.

In Section 2.2 the problem of collecting raw manufacturing information is dealt with in more detail.

2.2 General Concepts of Data Acquisition.

Broadly, *data acquisition* as used in the ensuing discussions will be taken to cover the reading, conditioning and transmission of information. Specifically, this information is confined to that generated by manufacturing processes such as temperatures, flow rates, machine speeds *etc.* In this case, the sources are divided into groups of those that produce information in analogue form such as thermocouples and those that are inherently pulse type such as piece counters. This information, although produced by predominantly physical processes such as pressure is assumed to be convertible for processing and transmission by electronic means. Thus a data acquisition system is assumed to include the distinct phases of sensing by transducers, signal conditioning of an electric signal from the transducers, its transmission and interpretation by a receiving device.

The character of the receiving device depends on the intended use of the acquired information. It may for example be a chart recorder showing continous curves of the behaviour of the monitored system or it may be an alarm watchdog which only reacts to unusual system behaviour or even a computerised monitor forming part of a supervisory and control system. However, a clear distinction is drawn here between data acquisition and control. Though a closed loop control system may possibly be built around the proposed D.A.S. this was not included as part of this research. The proposed D.A.S. was designed primarily as a monitoring system. Any consideration for extending it to be a building block of a larger application should therefore be taken in this light. In the remainder of this report it will be assumed that this is borne in mind.

The concept of real-time in data acquisition is interpreted here to mean that data captured from a process can be transmitted, processed and used to drive actuators that control the process as it happens. The term "*hard* real-time system" is often used [3] to define a system for which the performance

of the system does not only depend on the data's mathematical accuracy but also the time at which the results of computations are completed. In this case, the performance of the system clearly depends on the hardware devices used, the signal processing techniques and the computational software algorithms used. The software function is especially critical because it has a much larger time overhead than the operation of hardware. It is therefore the determining factor on the strict meaning of "real-time" and is task specific. That is, the pace of real events in time and the cost of their tracking error determine the precise meaning of *real-time* in each specific situation. For the designed D.A.S., "real-time" is intended to mean that the hardware is capable of responding to monitored events in real-time if user specified software is correspondingly designed to do so. For example, current practice at the CMB site is that oven temperature charts are replaced every 24 hours. On the other hand, one of the software routines used during D.A.S. tests outputs information every 5 minutes. In the context, the latter method may be considered to operate in real-time. It is therefore

left here for the D.A.S. user to define the concept of real-time and specify the software accordingly. We will hence dwell on the performance of the D.A.S. from a primarily hardware viewpoint. This will be done in Parts II and III. However, to aid in any future D.A.S. applications in *hard* "real time" situations we shall, as far as possible avail detailed timing information.

2.3 Operations at the CMB Site.

CMB Packaging Ltd, Thika started operations as the Metal Box Co. Ltd. in the 1950's. It was built essentially to meet the cans requirements of the then Kenya Canners (now Del Monte Kenya) Ltd. Later its interests expanded to supply other users of food cans, pvc pipemaking and security printing. Currently however, pipemaking has been discontinued. The site covers about 7 Hectares with the manufacturing centres concentrated over about 1/3 of the site. Operationally, can manufacturing and security printing are administered as completely different entities. The former is normally referred to as the Open-Top factory from the fact that its primary business is to make and sell open ended cans (accompanied by lids). Our main

concern in this project was the Open-Top operation.

There are four production centres: *Printing* where the raw material (plain tin-plate) is treated and decorated ; *Presses*, where can ends are made and *Canlines* where can bodies (cylinders) are formed, sealed at one end and the open-topped cans packed onto pallets. In these three areas, manufacturing information generated includes temperature, fluid flow rate, pressure, vacuum, fluid level, piece counting and machine speeds.

The fourth production centre is an ongoing attempt to consolidate commercial tool-making under the *Technical Services* department. This department has also made plans to manufacture production machinery and spares for related industries such as food canning.

The fifth source of manufacturing information are the utility services; bulk water, gas, vacuum, pressure, electricity *etc.* Rationalization of their production, distribution, efficient use and conservation is being taken increasingly seriously. For example, heat recovery in the Printing Department ovens is under consideration. A data acquisition

system monitoring these is important because currently no comprehensive monitoring or auditing is done. As such the rationalization mentioned above becomes difficult.

It will be seen from the foregoing discussion that a data acquisition method tried and found successful in one production centre should be easy to adapt for other centres. Secondly since all centres are inherently sequentially dependent, it would be extremely useful if they were linked for central monitoring by Management. This is the view agreed on during initial consultations over this project. The strategic implications of this are significant to the factory information structure as discussed in the context of Section 2.1. However at this point it is more useful to relate further preliminary technical background.

2.4 Current Data Acquisition Methods at the CMB Site.

Currently no comprehensive monitoring or data acquisition system exists for either any production centre or the overall manufacturing operation at CMB.

However it is standard that each production machine carries at least a minimum of monitoring devices fixed by its manufacturer. Thus for example an oven will have temperature monitoring facilities and a *bodymaker* a piece counter. These while convenient for use by the operators are grossly inadequate for either the manager overseeing the whole centre or the engineer analysing complete line behaviour. It will be useful at this point to go into some detail over this problem in the Printing Department where this project was based.

The physical layout of the Printing Department (hereafter referred to as *Printing*), is as shown in Fig. 2.1. The physical layout is important to a D.A.S. designer for several reasons. It determines the paths followed by signal lines to avoid obstacles, minimize noise coupling, ease installation and maintenance and minimize cable length. The layout also determines significantly the system architecture adopted by dictating the extent and physical location of signal processing and point-of-usage equipment. Before discussing the constraints introduced by the physical layout any further it is proposed to describe now the

activities and conditions in *Printing*.

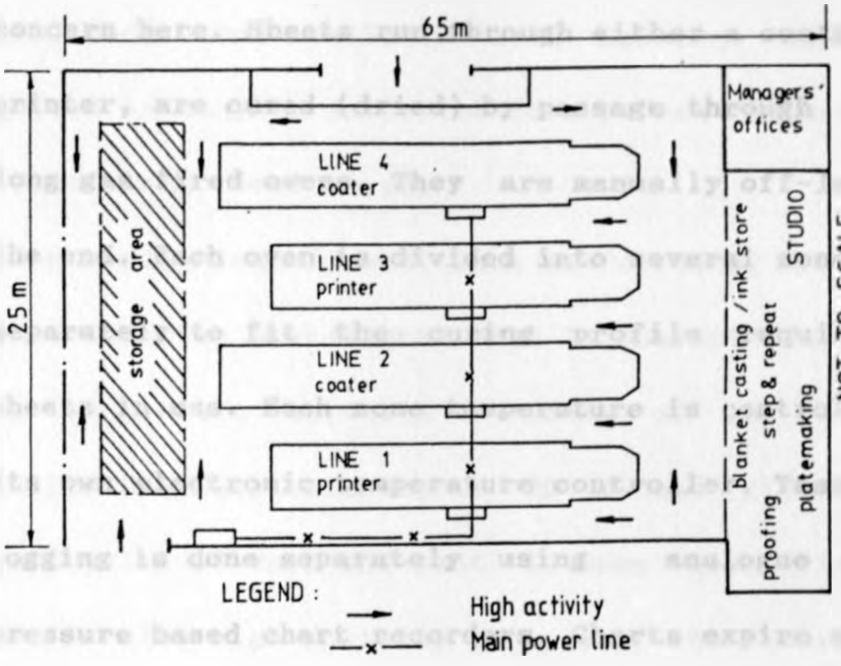


Fig. 2.1 Plan of the Printing Department.

The single objective of the Department is to apply various decorations and coatings on plain sheets of tinplate. This may be purely for decorative purposes or as anti-corrosion measures on the cans made later from the tinplate. Usually it is for both reasons. There are four production lines in *Printing*. Two are coaters and the other two are printers. The former apply coats of ink, lacquer or varnish over the

complete surface of a sheet. The latter are used to apply selected inks at precisely selected positions on a sheet *i.e. decorate* it. This distinction is of little concern here. Sheets run through either a coater or a printer, are cured (dried) by passage through 16 m long gas fired ovens. They are manually off-loaded at the end. Each oven is divided into several zones fired separately to fit the curing profile required for sheets in use. Each zone temperature is controlled by its own electronic temperature controller. Temperature logging is done separately using analogue mercury pressure based chart recorders. Charts expire every 24 hours.

The data acquisition need in *Printing* is typified by the requirements to monitor temperature (which is absolutely critical to the ultimate performance of cans), track batches of sheets in production (to reduce loss and mix-up) and archive centre information for future reference. This need is underlined by the fact that failure in any one of these areas has considerable cost penalties. The urgency of this need is prompted by the fact that the temperature chart recorders are obsolete and spares unavailable. Also,

the cost of supplying utilities such as water, gas, pressure and vacuum is rising so steeply that serious thought has to be given to their efficient use and conservation. (It is here that heat recovery is being considered). But reliable oven heating data is required in easy-to-interpret form before further work is done along those lines.

The environmental conditions in *Printing* are also noteworthy. The operational area is characterised by a wide temperature variation in excess of 20 $^{\circ}$C , a relative humidity going up to 80 % and significant accumulation of dust and soot. As seen from Fig.2.1, there is also high activity on most of the floor space precluding the positioning of the D.A.S. operator station there. Further, equipment in the working area must withstand wide temperature variations and tight ingress protection requirements. It is also significant that the department is installed with nearly fourty electric motors several of which are large (exceeding 10 kW). Also that power distribution in the department is not confined to a bus structure but tends to be grid-like. This raises the question of electromagnetic interference in signal lines, power

supply fidelity and electronic system protection. These will be revisited in Part II. Table 2.1 shows the current and projected data acquisition needs.

Table 2.1 Existing and projected monitoring in Printing.

TT TYPE	SIGNAL	EXIST./PROJ.	NO. OFF	TOTAL
Analogue	Temperature	Y / Y	12 / 8	20
,,	Flow	N / Y	0 / 12	12
,,	Utilities	N / Y	0 / 2	2
Pulse	Count /Speed	Y / Y	8 / 0	8
Reserve			2 per Line	8
TOTAL		Y / Y	20 / 30	50

It follows from the issues raised above that soon Management will need to make a decision on how best to deal with the problem of monitoring in *Printing*. The remainder of this report is dedicated to establishing and clarifying the important related facts and premises after which it proposes what appears to be the best way to deal with the monitoring problem in *Printing*.

PART II

Analysis

In this Part a systematic attempt is made to succinctly specify the data acquisition problem in the Printing Department. An analytically quantitative approach is invoked as far as possible. It is in this Part that the theoretical investigations are laid down and the question of the D.A.S. specifications tackled. Emerging at the end should be a clear picture of the kind of solution required and the proposed approach to its achievement.

CHAPTER 3

THE D.A.S. SPECIFICATION

In this chapter the theoretical basis for designing a data acquisition system for the Printing Department is addressed. This starts with a brief discussion of the physical constraints. Then a characterisation of the ovens as 2^{nd} order systems is presented. The question of the generality of the proposed D.A.S. for use on different process variables is also raised. To close Chapter 3, the process by which the specific D.A.S. architecture is arrived at is demonstrated. However these only cover the broad underlying concepts and mathematical treatment of the particular signal processing methods is deferred to Chapter 4. The objective here is to keep conceptual aspects from being obscured by mathematical detail.

3.1 Physical Constraints.

So far a qualitative picture of the Printing Department and its data acquisition problem has been presented. In this section, an attempt is made to

quantify both the ovens' behaviour and the requisite behaviour of the system to monitor them. Figs. 3.1 show typical oven responses to step changes of temperature set point. The curves shown were treated as typical and representative of the extremes of oven behaviour. They were thus used to arrive at the worst case design limits for the monitoring system. The curves were chosen as follows.

A visual inspection was initially done through all the charts collected over one year's operations. From these were selected two charts showing the most rapid rise and fall times for a step change in oven settings. One chart was selected showing oscillatory behaviour in the ovens. Some of these charts are reproduced in Appendix A.

It was expected that by analysing the responses of the ovens, a relationship can be made between their speeds of response and D.A.S. bandwidth and dynamic range specifications. Necessarily, the extremes of behaviour was used for this rather than attempt to arrive at the average response of the ovens and use it. This would imply that the D.A.S. would be out of specifications every time an oven

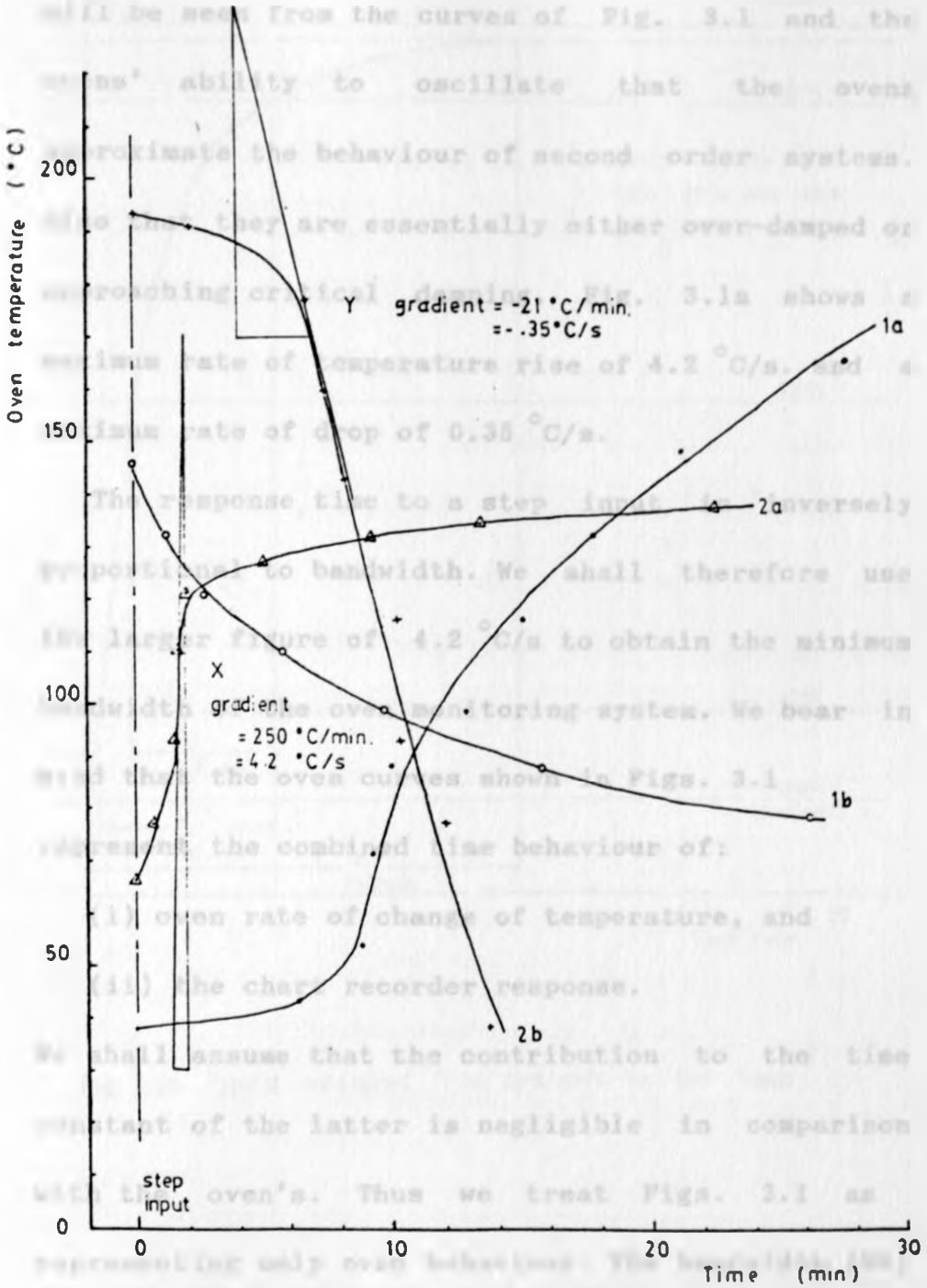


Fig. 3.1a Oven responses to step inputs

deviated slightly from the average behaviour. It will be seen from the curves of Fig. 3.1 and the ovens' ability to oscillate that the ovens approximate the behaviour of second order systems. Also that they are essentially either over-damped or approaching critical damping. Fig. 3.1a shows a maximum rate of temperature rise of 4.2 $^{\circ}$C/s. and a maximum rate of drop of 0.35 $^{\circ}$C/s.

The response time to a step input is inversely proportional to bandwidth. We shall therefore use the larger figure of 4.2 $^{\circ}$C/s to obtain the minimum bandwidth of the oven monitoring system. We bear in mind that the oven curves shown in Figs. 3.1 represent the combined time behaviour of:

(i) oven rate of change of temperature, and

(ii) the chart recorder response.

We shall assume that the contribution to the time constant of the latter is negligible in comparison with the oven's. Thus we treat Figs. 3.1 as representing only oven behaviour. The bandwidth (BW) of a monitoring system for the ovens must therefore have a rise time compatible with this. Because the design of transducers was not a part of this

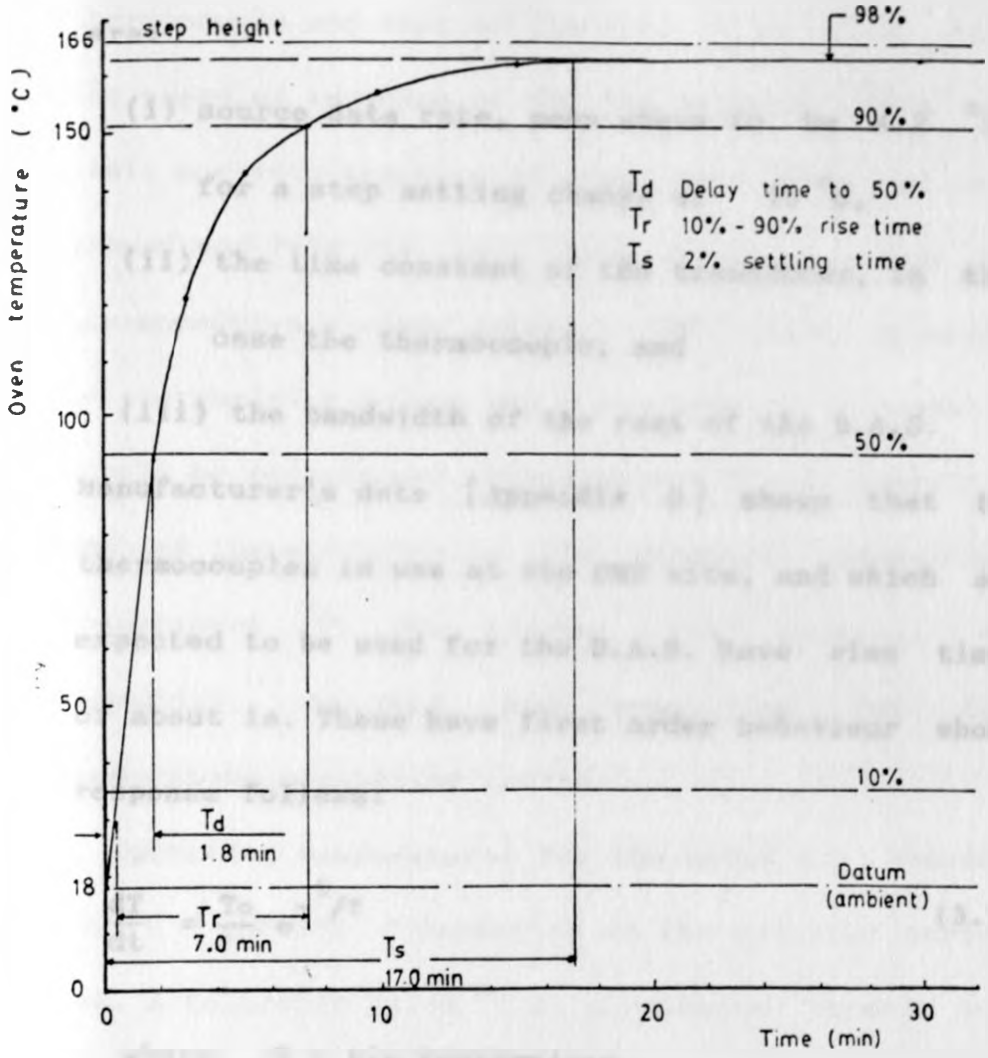


Fig. 3.1b Typical measured time constants for the ovens.

project, we distinguish here between three factors which affect the design as far as bandwidths are concerned with temperature monitoring. (Thermocouples are the already established

temperature sensors at the CMB site). These factors are:

(i) source data rate, seen above to be 4.2 °C/s for a step setting change of 75 °C,

(ii) the time constant of the transducer, in this case the thermocouple, and

(iii) the bandwidth of the rest of the D.A.S.

Manufacturer's data [Appendix B] shows that the thermocouples in use at the CMB site, and which are expected to be used for the D.A.S. have rise times of about 1s. These have first order behaviour whose response follows:

$$\frac{dT}{dt} = \frac{T_o}{\tau} e^{-t/\tau} \qquad (3.1)$$

where T = tip temperature,

To= temperature step input,

and τ = thermocouple time constant.

The maximum rate of rise of temperature after a step input to a thermocouple occurs at t=0. For a thermocouple of τ = 1s and a step input of 75 °C, $\max \frac{dT}{dt}$= 75 °C/s. (A step input of 75 °C is used to afford a comparison with the source data

rate in (i) above). Comparing the rise time of the thermocouple and that of the oven it is clear that the speed of response of the thermocouple does not limit accurate tracking of oven temperature. On this ground and from the fact that a large stock of thermocouples already exists at CMB, there appeared no overwhelming reason why a new type of transducer should be recommended. The proposed D.A.S. therefore adopted thermocouples as the standard temperature transducers. We now address the question of bandwidth, accuracy and resolution for the temperature monitoring system.

Operating temperatures for the ovens are between 148 $^{\circ}$C and 202 $^{\circ}$C depending on the specific curing job. A tolerance of +5 $^{\circ}$C is considered normal but that of -5 $^{\circ}$C undesirable. That is, over-stoving of up to +10 $^{\circ}$C are quite acceptable but any under-stoving is generally to be avoided. Fig. 3.2 shows the electrical characteristics for the thermocouples in this temperature range. It is seen that in this range, J and K thermocouples are for all practical purposes linear. The subjects of linearization and cold junction compensation will

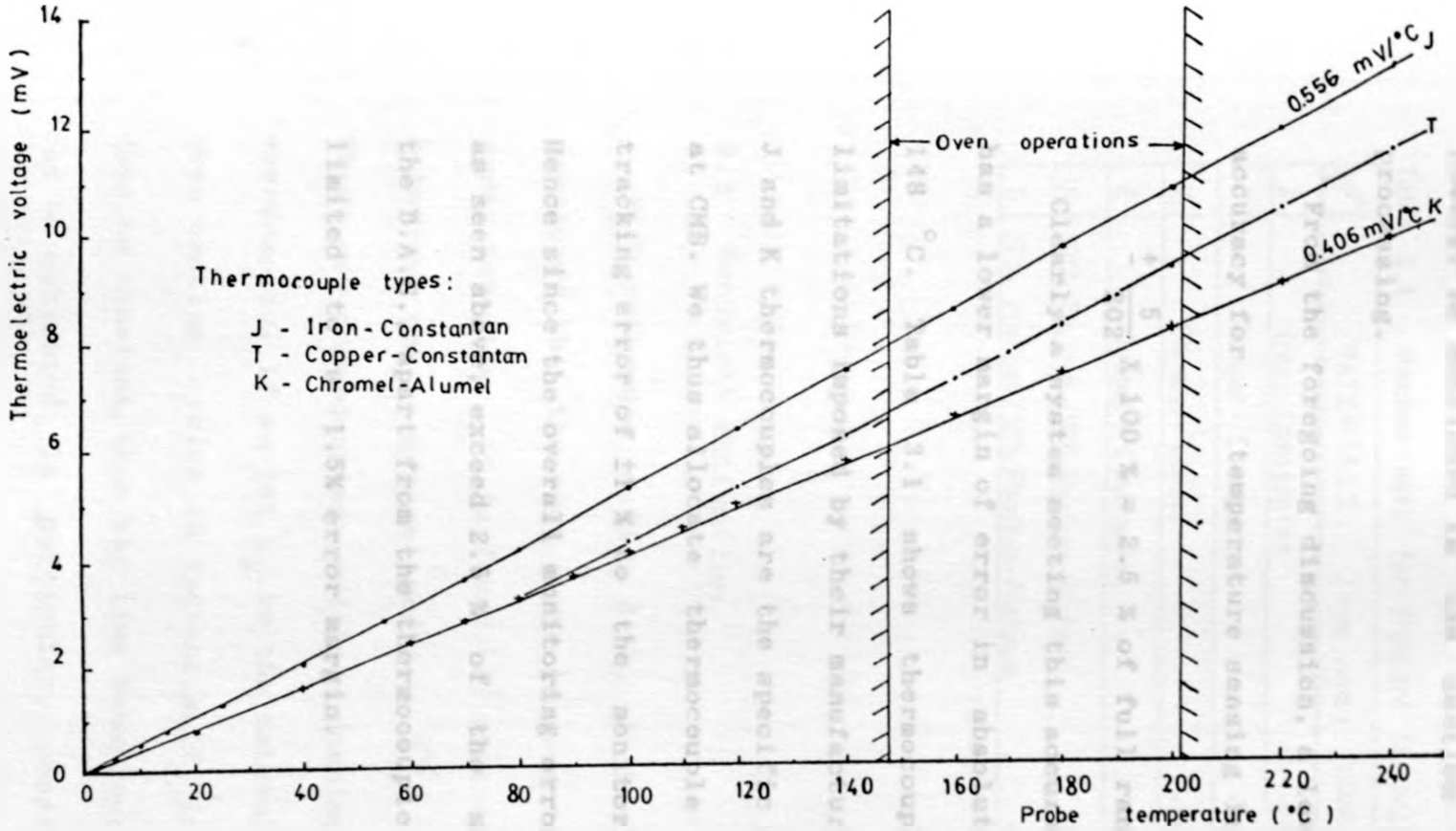


Fig. 3.2 Piecewise linearised thermocouple characteristics.

however be mentioned in the section under signal processing.

From the foregoing discussion, a lower range of accuracy for temperature sensing is obtained as

$$\pm \frac{5}{202} \times 100\ \% = 2.5\ \% \text{ of full range.}$$

Clearly a system meeting this accuracy at 202 ^{o}C has a lower margin of error in absolute degrees at 148 ^{o}C. Table 3.1 shows thermocouple accuracy limitations imposed by their manufacturing process. J and K thermocouples are the specific types in use at CMB. We thus allocate thermocouple temperature tracking error of ±1 % to the monitoring system. Hence since the overall monitoring error must not, as seen above, exceed 2.5 % of the set-point, the D.A.S., apart from the thermocouple should be limited to a 1.5% error margin.

Table 3.1 Nominal data for standard thermocouples. [29]

Type	MATERIALS (+ve, -ve)	USUAL RANGE °C	Error
J	Iron - Constantan	-190 to 760	±1
T	Copper - Constantan	-200 to 371	±5
K	Chromel - Alumel	-190 to 1260	±75
E	Chromel - Constantan	-100 to 1260	
S	90% Platinum/10% Rhodium - Platinum	0 to 1482	
R	87% Platinum/13% Rhodium - Platinum	0 to 1482	

3.2 Bandwidth Estimation.

With reference to Fig. 3.1b, it has already been mentioned that the oven curve is seen to approach 2^{nd} order behaviour. It is found [4] that three cases of behaviour can be generalised for 2^{nd} order systems. These are underdamping, critical damping, and overdamping. If we let ω_o be the natural frequency of oven heating cycles in radians/s (f_o in Hz), k be the damping constant, then the time behaviour of the oven can be estimated. In particular, consider the oven curve shown in Fig. 3.1b. It can be shown [4] that for this over damped case the temperature T may be expressed as

$$T(t) = \frac{1}{\omega_o^2}\left\{1 - \frac{1}{2}\sqrt{(k^2-1)}\left[-\frac{1}{k_1}\exp -(\omega_o k_1 t) - \frac{1}{k_2}\exp -(\omega_o k_2 t)\right]\right\}$$

where $k_1 = k - \sqrt{(k^2-1)}$,

$k_2 = k + \sqrt{(k^2-1)}$ and

$k > 1.$ (3.2)

Shinners [4] shows that the 98% settling time, T_s of a 2^{nd} order system is given by $T_s = 4/\omega_o k$. Applying this to the curve of Fig. 3.1b with T_s = 17 minutes, we get

$$f_o = 6.24 \times 10^{-4}/k \quad \text{Hz.}$$

We use k = 1 to give $f_o \cong 6.2 \times 10^{-4}$ Hz by assuming that Fig. 3.1bis critically damped. Thus we have f_o = 6.2×10^{-4} Hz. (Micheletti [5] shows an alternative approach to this problem).

Now consider that Fig. 3.1a shows that the maximum rate of change of temperature is 4.2 °C/s. Suppose this change is taking place somewhere in the oven operational range between 148 °C and 202 °C . To achieve a monitoring error of at most 1.5 % of the

actual temperature, the monitoring system must resolve the sample readings to at least 2.2 °C at 148 °C and 3 °C at 202 °C. Choosing the resolution of 2.2 °C as the determinant, then a temperature changing linearly at 4 °C /s must be read at least twice every second. This calls for a sampling clock of at least 2 Hz.

This discussion has so far tried to establish two things : the characteristic of a typical oven in terms of its natural frequency and in terms of its transient response to a step change. As transient behaviour is critical to the understanding of abnormal conditions on the ovens, it is proposed that some capacity to monitor it be included in the D.A.S. Thus D.A.S. design assumes that oven temperatures are signals of at least 2 Hz in bandwidth.

The next question concerns pulse outputs in Printing generated by counting devices. These may be piece counters or machine speed monitors. The maximum rated speed of the ovens is 6000 sheet passes an hour or approximately 1.7 sheets a second (s.p.s.). The counting pulses generated can be filtered to produce a sine wave at the counting frequency. Thus in the D.A.S. design, sheet counting is taken to source

signals of at most 1.7 Hz.

The last question relates to the bandwidth of the monitoring system. It may be intuitively evident that the baseband signals involved are unlikely to exceed the bandwidth capacity of an average electronic system. But this question is still of interest because monitoring systems will sometimes apply non-electronic techniques. The fastest rise-time of the measured signal and the degree of acceptable tracking error determine the maximum acceptable rise time of the monitoring system. If n is the maximum percentage error allowed in measuring the signal of rise time t_r then the measurement system must have a rise time t_m of at least [6],

$$t_m = \sqrt{[(1+n/100)^2-1]}\, t_r \qquad (3.3)$$

Thermocouples have been stated above to have inherent inaccuracy of about 1% . Suppose future development improves this to 0.1%. For the oven of Fig. 3.1b , t_r=420 s. Under these conditions, we specify a D.A.S. whose frequency response will then limit the overall monitoring function no more than the primary transducer itself. We thus use n=0.1% for the

D.A.S. to get its rise time t_m as t_m=18.8 s. The 3 dB bandwidth BW of such a system can be shown [6] to be given by BW = 0.35 /t_m = 1.9 X 10^{-2} Hz.

This bandwidth would be sufficient to monitor normal oven operation. However it has already been explained how a working bandwidth of 2 Hz was arrived at. To introduce scope and flexibility to the monitoring system it was decided that all channels be assumed to have a bandwidth of at least 10 Hz. By the procedure outlined above (eqn.3.3), the nominal D.A.S. bandwidth was thus specified to be 250 Hz. Since this particular system is all electronic this requirement is considered exceedingly liberal and no further attempt is made to pursue the issue analytically.

Although temperature and counting are the two signal sources covered here in detail, it is taken that an extension of the analysis for other variables is straight forward. In the discussion following in Section 3.3 , it will be explained why the specific variable being monitored makes very little difference to the overall design and operation of the D.A.S.

3.3 A Discussion of the Architecture of the D.A.S.

The issues related to the selection of the D.A.S. architecture are transducer selection, extent and location of signal processing, general signal format and the actual topological layout.

A distinction has already been made between the two basic types of signal sources dealt with, namely analogue and pulse. It has also been explained that currently the former arise from thermocouples and the latter from counting sensors. A decision was made as explained earlier, to use the already existing transducers for any future monitoring system.

Signal processing is necessary because raw transducer signals may need to be intelligibly interpreted. They may also have to be processed against the effects of noise either near the signal source or during transmission. The real question is not quite whether the signals need to be processed but rather where and how in the system this should take place. From the layout drawing of Fig. 2.1 of the Printing Department it was stated that high activity on the shop floor necessitates that the D.A.S. output point be located elsewhere. This is especially so

because at this point sensitive equipment such as a computer and its peripherals may be in use. It is therefore clear that signal transmission over at least 100m from source must be considered. The signals therefore have to be processed to deal with channel noise. Processing the signals at the source makes it easier to reduce the effect of noise in the received signal. But in this case it means more sophisticated circuitry at the system front end than if raw signals are transmitted.

In the case of the CMB site, the conditions at the signal sources are quite harsh as explained earlier in Section 2.3. Space is also limited. It was therefore proposed that only minimal signal conditioning be done at the transducer location to keep the circuitry uncomplicated and robust and save space. The electronics units designed to achieve this are referred to here as transducer-transmitters (TT) and qualified with A or P for analogue and pulse types.

The next decision was in regard to transmission topology. The choice existed between wiring all the TT units to the central receiver 100m away or alternatively introducing an intermediate unit/s to

load them onto a single link to the receiver. These two possibilities are shown in Fig. 3.3. These two schemes are considered to be significantly different as to have important implications to D.A.S. implementation. They are qualitatively explored below for the five factors of expected performance, design, installation, operation and cost. The analysis assumes a general system with a large number of TT's and from

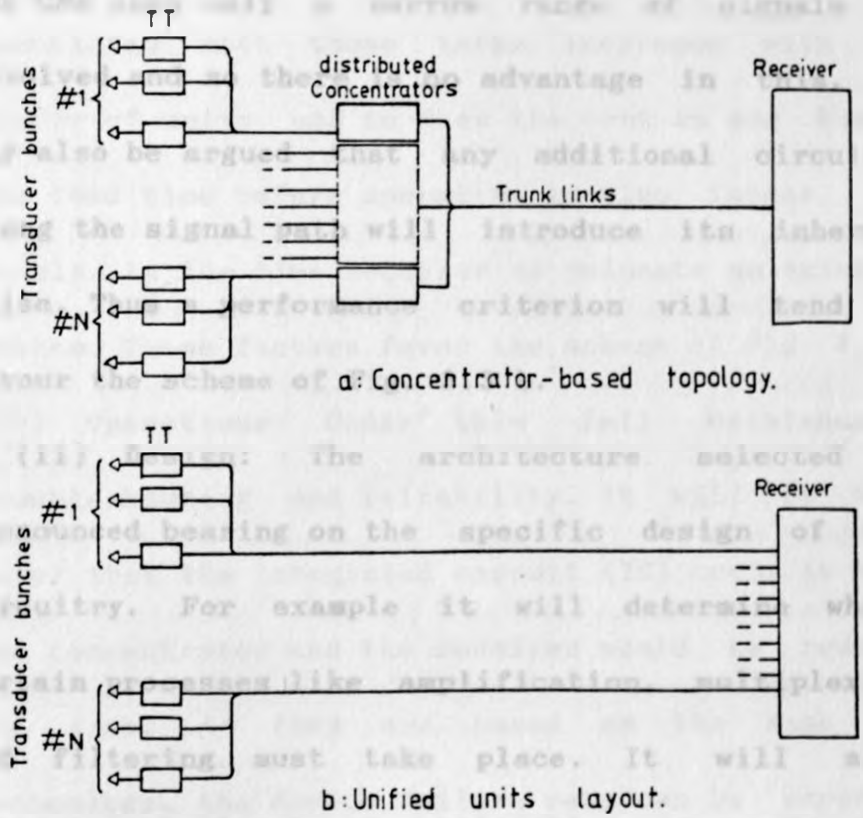


Fig. 3.3 Two options for D.A.S. architecture.

which the CMB set up is drawn out as a special case.

(i) Expected performance: This relates to the anticipated effects of such factors as electrical noise, mechanical vibration and the physical environment on system reliability. The architecture of Fig. 3.3a, because it is more decentralised offers the chance of uniquely specifying the concentrator to fit optimally with a specific type of signal bunch. However it may be argued that in the CMB case only a narrow range of signals is involved and so there is no advantage in this. It may also be argued that any additional circuitry along the signal path will introduce its inherent noise. Thus a performance criterion will tend to favour the scheme of Fig. 3.3 b.

(ii) Design: The architecture selected has pronounced bearing on the specific design of the circuitry. For example it will determine where certain processes like amplification, multiplexing and filtering must take place. It will also determine the level of utilization of particular circuits. For example while the scheme of Fig. 3.3a will require some kind of multiplexer for each

concentrator, Fig. 3.3b requires only one. However, from an overall viewpoint the same actions have to be performed in the D.A.S. irrespective of the location at which they are done. Thus the circuitry remains essentially the same irrespective of its physical position. Hence the level of design complexity is roughly the same for either scheme.

(iii) Installation: This covers the technicalities of running signal and power lines and physically mounting the electronic units. The difficulty associated with these tasks increases with the number of units and so does the cost in man hours. The lead time before operation is also longer. And so also is the time required to relocate an existing system. These factors favor the scheme of Fig. 3.3b.

(iv) Operations: Under this fall maintenance, troubleshooting and reliability. It will be seen later that the integrated circuit (IC) count in both the concentrator and the receiver would be roughly the same. As they are based on the same IC technology, the device failure rate can be expected to be almost the same. This implies that for the overall system, the distributed scheme may be expected to be partially non-functional more often.

On the other hand single failure in the centralized system of Fig. 3.3b is also more likely to cripple the whole system. Nevertheless the centralized system will be easier to troubleshoot because it is self contained and more easily accessible for maintenance. Thus from the view of operations, a centralized system appears more favourable although it implies greater concern with system reliability from design to maintenance.

(v) Cost: Hardware costs are treated separately from all the others because they are more amenable to quantification. Fig. 3.3 is used in the attempt to do this. It will be seen that both schemes have the same layout up to the imaginary point where the concentrator is fixed.Hence the analysis covers only the link from this point to the receiver. We consider the three big contributors to hardware costs; cable and conduit cost, mounting and the effect of duplication of circuitry. From Fig. 3.3, let

N = number of transmitter bunches or concentrator units,

T = average number of transducers per bunch, and

l = average length of electrical path from concentrator to receiver.

If concentrators are used, the one way total length of wire used is

$$L_c = Nl \tag{3.4}$$

If all TT wires run to the receiver, so that no concentrator is used, the one way total length of wire is

$$L_r = TNl \tag{3.5}$$

We now break down the system costs.

(a) Wire and conduit costs:

The values L_c and L_r also represent conduit lengths. In all cases where $T \geq 1$ the wire plus conduit cost if there is no concentrator will exceed the cost when one is used by the difference between equations (3.4) and (3.5).

i.e $$C_{dw} = NlC_w(T-1) \tag{3.6}$$

where C_w is the cost of unit length of wire plus conduit.

(b) Installation and mounting:

The laying of conduit, pulling of wire and mounting of the units is expensive in materials and labour. If no concentrators are used then only one unit

(the receiver) will be mounted, say at a cost C_m but if concentrators are used then for N of them the cost will be NC_m. The cost difference for mounting, assuming like in (a) that the latter is less, is thus

$$C_{dm} = -C_m(N-1) \qquad (3.7)$$

(c) Duplication:

Duplication arises because certain circuits (*e.g.* power supplies, packaging boxes *etc.*) are repeated for each concentrator while only one of each is used if no concentrators are used. Thus the scheme of Fig. 3.3b cannot be treated strictly as a purely compacted version of Fig. 3.3a. Usually, the power supply and packaging costs contribute very significantly to the product cost. In this case it is found that the cost of the concentrator is very nearly equal to the cost of the receiver if as is true here, the IC count and circuitry complexity are of the same order. Let C_d be the unit cost of a concentrator, then a duplication cost difference C_{dd} can be defined by which Fig 3.3b exceeds 3.3a *i.e.* $C_{dd} = -C_d\ (N-1)$. (3.8)

The total cost difference , C_T, between the two

schemes is thus the sum of C_{dw}, C_{dm} and C_{dd}. That is,

$$C_T = NlC_w (T-1)-(N-1)(C_m + C_d). \quad (3.9)$$

If C_T is negative, then it is cheaper not to use concentrators and vice-versa. Below we isolate two cases of interest.

(i) Large system : $N \gg 1$, $T \gg 1$, hence

$$C_T = N(lTC_w - C_m - C_d).$$

The break point for which to use or not to use a concentrator is reached at $C_T=0$ *i.e.*

$$C_w lT \begin{matrix} U \\ \gtrless \\ D \end{matrix} C_m + C_d. \quad (3.10a)$$

Equation (3.10) is a costs equation with the left hand side representing installation cost and the right hand side the costs associated with each installed unit. "U" stands for "use a concentrator ", "D" for "do not". A second interpretation of equation (3.10) is that there exists a critical separation l between source and receiver for which it is cheaper to use a concentrator. Further, from equation (3.9), the cost advantage of using concentrators increases linearly with l for large l.

(ii) The CMB case: Assume that transducers in Printing are bunched together according to production

lines *i.e.* N=4. Also as is seen in Table 2.1, T=13. Hence applying equation (3.9) and considering that in practice $C_m \ll C_d$ then in this case equation (3.9) simplifies to

$$l \leq \frac{3C_d}{48C_v} \cdot \qquad (3.10b)$$

It was also found in practice that C_d is about three orders of magnitude above C_v (*i.e.* total cost of concentrator devices affected by the duplication factor verses the unit cost of wire plus conduit). Using $C_d/C_m = 10^3$, we get an estimate of the break length for the CMB case as

$$l \geq 62.5 \text{ m}. \qquad (3.11)$$

In this case it was found that l as dictated by the physical layout of the factory exceeds 62.5 m and a concentrator unit was used as in Fig. 3.3a. Consequently the D.A.S. architecture that emerged consists of small transducer -transmitter units feeding into an intermediate concentrator/multiplexer unit. This in turn is connected by a single link to the receiver unit. Next is the question of what specific signal transmission techniques to use. This is the subject matter of the next chapter.

CHAPTER 4

SYSTEM CHOICE AND EXPECTED PERFORMANCE

This chapter discusses the various issues related to choice of the signal transmission schemes to be used . It then summarises facts relating to noise effects considered significant. Following this, the expected performance of the various transmission schemes is analysed and firm choices made between them. The last section deals with the details of the processed signals themselves and the link performance. Because quantitative system performance indicators are developed progressively in the discussion, they are scattered throughout this chapter. Chapter 5 is a concise restatement of the most important parameters derived in this chapter.

4.1 Choice of Transmission Schemes.

In previous sections it has been stated that signal sources may be expected to be analogue or pulse-types. It appears reasonable however that one mode of transmission through the D.A.S. must be selected to

simplify its design. We break down the D.A.S. into a front end (transducer to concentrator) and rear end (concentrator to receiver). A choice must be made between analogue and pulse/digital transmission for each half. We consider first the front end.

Digital transmission avails easier circuit design, better circuit performance predictability and possibility of data coding for error detection and correction. However it also requires increased bandwidth. It is also difficult to operate in the kind of hostile environment existing in the Printing Department. On the other hand, although analogue circuitry is harder to design, it is easier to make more rugged. The space available at the transducers makes it very desirable to have small TT units. This requires that only minimal signal processing be performed by these units. There is therefore little chance to install sophisticated digital units to take advantage of its versatility in signal handling. Due to these considerations, analogue transmission was selected for the front end. To determine whether analogue baseband or carrier-modulation front end transmission should be used one technique of each

method was selected. A comparison between the two methods was made in order to arrive at a decision.

The two transmission techniques considered were linear current loop (CL) transmission and frequency modulation (FM). CL was considered on the grounds that in an environment such as was being considered, many interference voltages can be expected, making voltage signaling intuitively unattractive. A current signalling scheme appeared preferable. This was reinforced by the fact that a popular technique like this exists and CL is a virtual industrial standard [7]. In this instance a source signal is used to vary the current flowing in a current loop connecting the source to the receiver . The receiver simply measures the current in the loop to determine the transmitter signal level. CL was chosen as the most preferred baseband analogue transmission scheme.

FM was chosen as the preferred analogue carrier modulation scheme for consideration. Although in order of noise performance FM is considered generally inferior to phase modulation (PM), its attraction lies in its simpler implementation [8]. Thus in Section 4.3 the baseband CL and modulation FM

schemes will be analytically compared. From this CL transmission will be shown to be preferable for the front end.

Consider now the choice of the method by which signals from the concentrator travel over the single link to the receiver. For the rear end digital transmission is overhelmingly more attractive. This is because the concentrator unit by its basic functions demands complicated circuitry which is easier to design and test if it is digital. Also because at this point it is a great deal easier to apply the error limiting advantages available in digital transmission. Finally since the receiver end is ultimately required to be compatible to digital equipment such as printers and computers it is easier to design it as a completely digital unit. Consequently digital transmission is used in the rear end. The concentrator unit is therefore a hybrid of analogue and digital circuits as it is the interface between the front and rear ends.

Digital transmission may take place at baseband or by use of modulation techniques. The selection of the method to be used at the rear end is deferred until

after the discussion of noise in the next Section.

4.2 Noise.

Two kinds of electrical noise are considered here: intrinsic system noise and externally induced (extrinsic) noise. It is not intended that mathematically rigorous treatments be pursued, rather that the effects of noise on the system be put into proper perspective. The intrinsic noises considered are *thermal*, *1/f* and *shot* noise. External noise mentioned are the electromagnetically coupled interference (EMI) including impulse noise and mains conducted noise.

Intrinsic Noise.

(a) Thermal noise.

This results from random motion of electrons in a conductor and is an intrinsic property of all resistive devices. It is also referred to as Johnson noise and has an equal power at all frequencies. It is "white " and Gaussian noise with thermal noise r.m.s. voltage is given by [9]

$$e_t = \sqrt{4kTBR} \qquad (4.1)$$

where k = Boltzmans constant = 1.38×10^{-23} J/ $^{\circ}$K,

R = resistance across which the noise is measured,

B = the bandwidth under consideration,

and T = the absolute temperature of the resistor in Kelvin:

similarly the r.m.s. thermal noise current is given by

$$i_t = \sqrt{4kTB/R} \ . \qquad (4.2)$$

In general, a resistive two terminal network having all resistors at the same temperature produces an r.m.s. open circuit thermal noise voltage equivalent to that generated by a single imaginary resistance as seen looking into the network. Purely reactive elements do not contribute to thermal noise. However in a network with reactive elements, the equivalent impedance $Z(f)$ is frequency dependent and expressible in terms of equivalent reactance $X(f)$ and resistance $R(f)$ *i.e.*

$$Z(f) = R(f) + jX(f) \qquad (4.3)$$

R(f) therefore replaces R in equations (4.1) and (4.2). But for frequencies in use at the D.A.S. front end this dependence of R on frequency can be ignored. Equations (4.1) and (4.2) are therefore directly applicable.

(b) 1/f (Flicker) Noise.

This type of noise is of significance in active devices operating at low frequencies, f. The noise power related to it increases as 1/f. It has been associated with the terms "contact noise" and "excess noise" depending on its various manifestations in electronic devices and circuits. Fig. 4.1 shows the distribution of noise intrinsic power over frequency. 1/f noise is said [10] to dominate the noise properties of active devices up to about 10 kHz above which shot and thermal noise predominate. It has also been found that well designed transistors will typically generate negligible 1/f noise above 1kHz but having no known lower frequency limit [10, 11].

The law governing the variation of current, i_f generated by 1/f noise is given by [9]

$$i_f = \sqrt{\frac{KI^{\beta}}{f^{\alpha}} \Delta f} \qquad (4.4)$$

where K = a constant,

I = dc current through the device output terminals,

f = frequency at which noise measurement is taken,

α = a constant near unity (usually $0.7 \leq \alpha \leq 1.3$),

β = constant of the order of unity (usually $\cong 2$),

and Δf = incremental noise bandwidth considered about f.

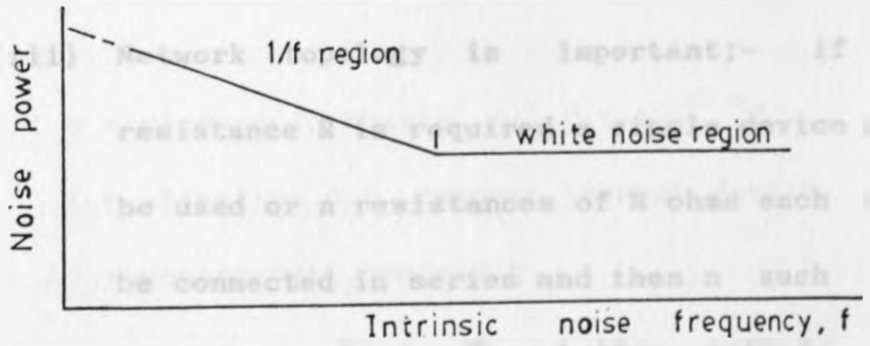


Fig. 4.1 Noise contribution in circuits [10].

1/f noise is non-Gaussian and there is no one

generally accepted theory of its mechanism to allow purely theoretical prediction of its magnitude because some of the parameters of eqn. 4.4 are empirically obtained. It is usually just measured [10] if its value is required. Nevertheless van del Ziel [11] and Bell [10] give some useful hints for its minimization in system design. These include:

(i) System operating frequency;- should be as high as possible.

(ii) Device choice;- carbon, metalised and wirewound resistors produce 1/f noise decreasing in that order.

(iii) Network topology is important;- if a resistance R is required a single device may be used or n resistances of R ohms each may be connected in series and then n such strings paralled. The latter method reduces 1/f noise by a factor of n^2.

(iv) Choice of noise breakpoint;- the frequency at which 1/f noise is considered significant is the corner point at which it equals thermal noise and below which it increases as 1/f. For bipolar

transistors this is in the region of 100 - 1000 Hz and 10 kHz - 50 kHz for FETs and GaAs MESFETs respectively.

(c) Shot Noise.

This arises because of the discrete nature of charge flow and appears in most active devices. It is also referred to as Shottky noise. Shot noise is "Gaussian" distributed in amplitude and "white " in frequency content. Its r.m.s. value i_s, at the output of a device is given by [9]

$$i_s = \sqrt{2qI\Delta f} \qquad (4.5)$$

where q = electronic charge = 1.6×10^{-19} °C,

I = effective d.c. current through device,

and Δf = measurement bandwidth.

Extrinsic Noise.

Although there are natural and man-made sources of externally induced noise it is assumed here that the latter predominates in the industrial context. This noise generally interferes with desired signals either

by coupling onto signal lines or reaching the system by conduction through power lines. The latter is covered as a practical detail in Part III. The following discussion is centred on the EMI coupling to signal lines.

This noise may be considered in two categories - continuous and random impulsive interference. The continuos radiation arises from the flow of large currents ; especially from power supply lines to heavy machinery on the shop floor. It will also originate from the normal regular function of the machinery. Examples include sources such as brush, slip ring and sparking action on rotating machinery and harmonics arising from the electrical and mechanical asymetry of the machines. This continuous form of electrical noise is conducted in the power distribution network or is otherwise radiated at conductor discontinuities such as distribution points and switchgear. Its frequency content is essentially made up of line frequency harmonics [12].

Random impulsive radiation is constituted of very short duration high level spikes of electrical energy that couple to the signal. They have a relatively flat

frequency spectrum. Therefore for twin wire transmission of a bandwidth of say 250 kHz impulse noise is seen as white noise.

Flourescent lamps also generate EMI due to plasma arc currents. The noise is evident in the band 500 kHz - 200 MHz [12] and will therefore not concern transmission over the 250 kHz bandwidth wire pair.

Ficchi [12] has stated that the continous overall noise components in a typical factory set up are only significant below 1 MHz peaking at 300 kHz and falling off at about 24 dB/octave above that. A graphical illustration of this is shown in Fig. 4.2. In [9] it is explained that the Poisson distribution is the basic phenomenon describing impulse noise. Further, it can be shown [13] that as the number of sources (trials) increases, the Poisson distribution tends to the *Normal* (Gaussian) distribution. It appears reasonable therefore to assume that in a shop floor with several dozen motors controlled by several hundred randomly switching devices, noise spikes will approach a Gaussian distribution. Thus a proposition is made that in the first instance the impulse noise arising in the Printing Department may be treated as additive white

and Gaussian. Although a lack of equipment made it impossible to measure the actual levels of this noise, it will be shown in Section 4.4 that this is not a major handicap to the analysis. Practical measurements of continous noise coupling onto signal lines produces the curves shown in Fig. 4.3. with a *real r.m.s.* meter used to give r.m.s. values.

In Sections 4.3 and 4.4 we analyse quantitatively the effects of the various noises mentioned above recalling that at the front and rear ends analogue and digital transmission are used respectively.

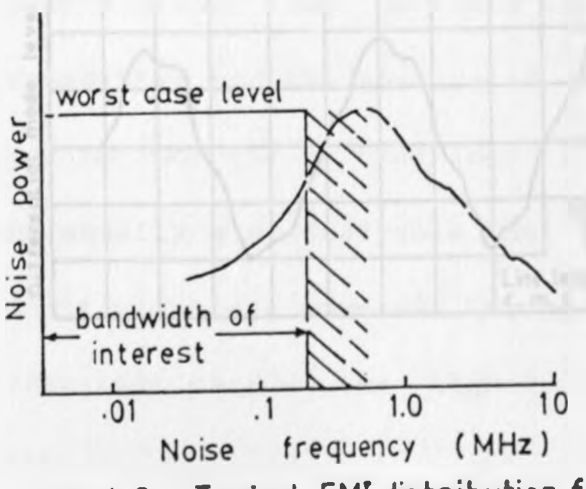


Fig. 4.2 Typical EMI distribution for factory [12].

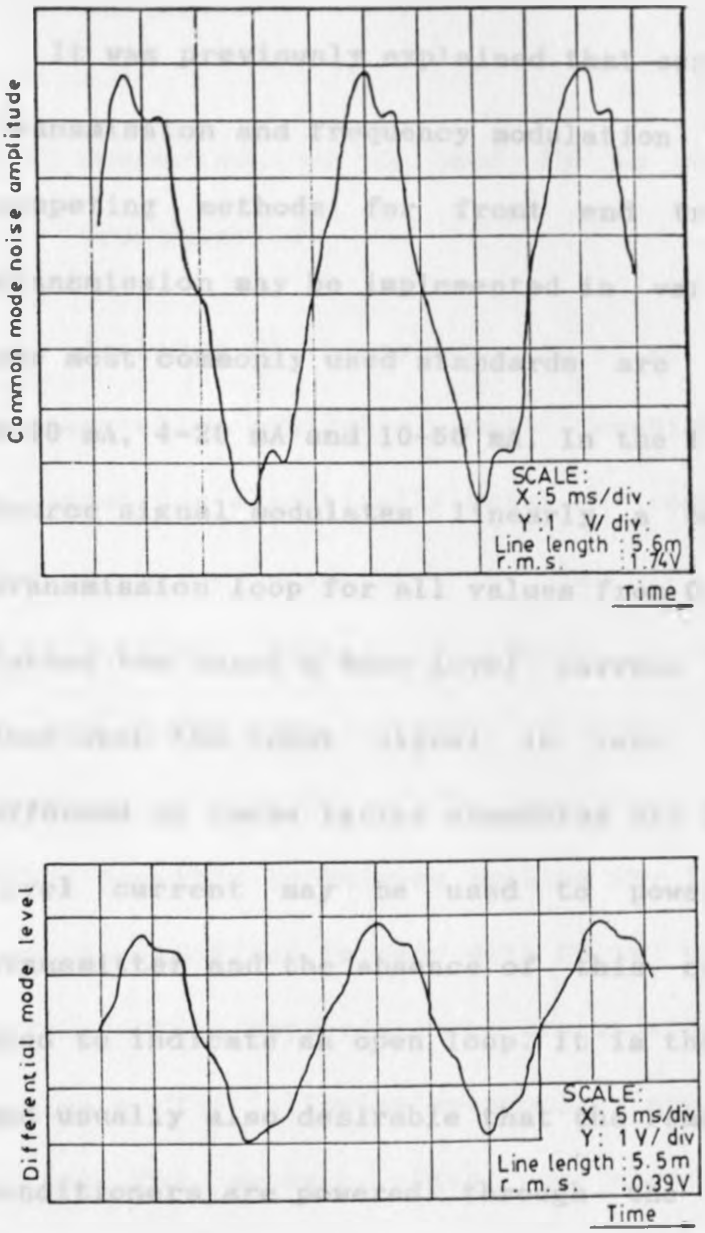


Fig. 4.3 Measured noise waveforms in Printing.

4.3 Analogue Transmission.

It was previously explained that current loop (CL) transmission and frequency modulation (FM) were the competing methods for front end transmission. CL transmission may be implemented in various ways but the most commonly used standards are the so called 0-20 mA, 4-20 mA and 10-50 mA. In the first one, the source signal modulates linearly a current in the transmission loop for all values from 0-20 mA. In the latter two cases a base level current flows in the loop when the input signal is zero. The advantage afforded by these latter standards are that this base level current may be used to power the remote transmitter and the absence of this current can be used to indicate an open loop. It is therefore common and usually also desirable that the remote transducer conditioners are powered through the same pair of wires that carries the signal. This reduces system cost.

FM is a widely documented [8, 14, 15] carrier modulation technique for analogue signal transmission. In FM, signal information is transmitted by the frequency properties of a carrier waveform. To follow

now is a brief discussion of the performance of these two techniques.

4.31 Comparison of CL and FM in analogue signal transmission.

Analogue CL transmission is often an option in commercially available data acquisition systems designed for electrically noisy environments [15]. It has a major advantage in that it uses baseband transmission, making it easier to implement than carrier modulation systems. However one needs a quantitative measure of its comparative performance to other possible techniques such as FM. In this section such a comparison is made with FM in pertinent noise effects. Some approximations are made to simplify the analysis. The following assumptions are also used:

(i) The message signal is slowly varying in comparison to external noise effects.

(ii) Extraneous channel noise has negligible power in the bandwidth B of the message signal $m(t)$. As such the limiting noise effects after low-pass filtering in the CL system, are intrinsic to the loop. These effects are: thermal, shot and 1/f noise.

(iii) Loop impedance parameters vary negligibly in time as compared to $m(t)$; channel linearity is also assumed.

(iv) The FM carrier frequency f is much greater than B and lies in the spectrum of the externally induced noise. As such, additive white *Gaussian* noise (AWGN) is predominant in FM.

a. Performance of CL transmission.

Consider the CL scheme where a remote transducer-transmitter sends information by varying the current it sources and sends through the loop. The receiver incorporates a device that measures this current and decides what the value of $m(t)$ is. Let the total loop current be $I(t)$ such that

$$I(t) = I_o + k\, m(t) \qquad (4.6)$$

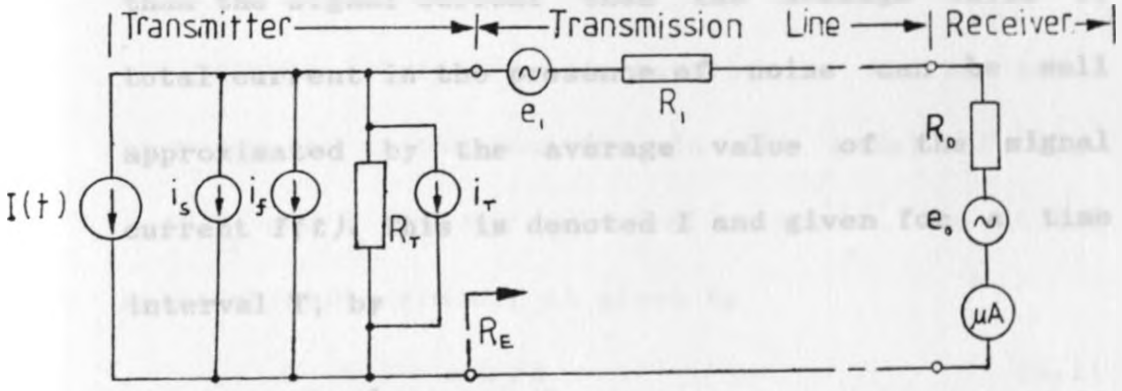
where, I_o is a constant current for $m(t)=0$,

k is a constant of proportionality and

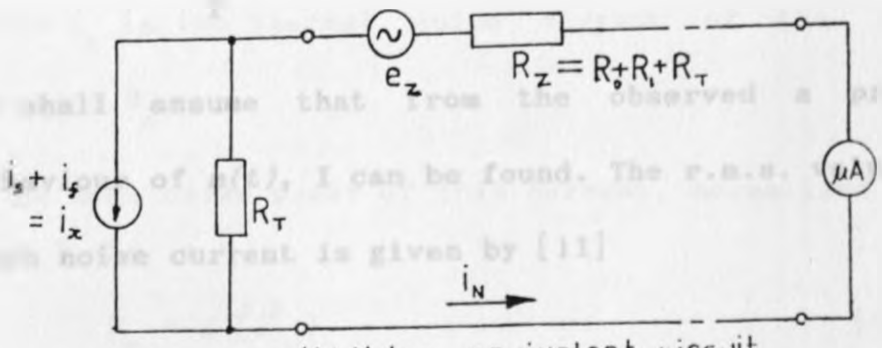
$m(t)$ is the input message signal, $0 \leq m(t) < \infty$.

So long as I_o is constant and known as the current when $m(t)=0$, it can be corrected for. It plays no

further role in the ensuing analysis where we shall assume $I(t) = k\, m(t)$. A low frequency circuit model is adopted and the loop resistances are as shown in Fig. 4.4a. The receiver is represented by its *Thevenin* equivalent and the transmitter by the *Norton* equivalent. Fig. 4.4b shows a simplified version of Fig. 4.4a for only the noise components.



(a) Complete CL circuit.



(b) Noise equivalent circuit.

KEY:

current source — microammeter

e.m.f. source — resistor

Fig. 4.4 Conceptual models of CL noise.

The parameters are

R_o = receiver input resistance,

R_z = lumped resistance of the complete loop,

$i_x = i_s + i_f$ *i.e.* r.m.s. shot and 1/f noise currents and

e_z = thermal r.m.s. noise voltage of R_z.

It is known [11] that both i_s and i_f noise currents depend on the average or d.c. value of the signal current. If all these noise currents are much smaller than the signal current then the average value of total current in the presence of noise can be well approximated by the average value of the signal current $I(t)$. This is denoted I and given for a time interval T, by

$$I = \frac{1}{T}\int I(t)\ dt. \tag{4.7}$$

We shall assume that from the observed *a priori* behaviour of $m(t)$, I can be found. The r.m.s. value of each noise current is given by [11]

$$i_s = \sqrt{(2qI\partial f)}\ , \tag{4.8}$$

$$i_f = \sqrt{(KI^b\partial f/f^\alpha)}, \tag{4.9}$$

$$i_z = \sqrt{(4kT\partial f/R_z)}, \qquad (4.10)$$

where, q is the electronic charge, 1.6×10^{-19} C.,

∂f is the bandwidth over which the noise is measured,

K is a constant,

b is a constant of the order of unity ($b \cong 2$ [11]),

α is a constant near unity ($0.7 \leq \alpha \leq 1.3$ [10])

k is Boltzmans constant, 1.38×10^{-23} J/°K, and

T is the absolute Kelvin temperature of the resistance R_z.

Assume that current sensing is by an ideal microammeter at the receiver. In the model of Fig. 4.4b R_T and R_z are now noiseless resistors. The total noise current, r.m.s., is given by

$$i_N = i_z + i_x R_T/R_z \qquad (4.11)$$

where i_z is the thermal noise current of the loop resistor R_z.

The mean noise power of this current, normalised into 1 ohm is

$$P_N = E\{i_N^2\} \qquad (4.12)$$

where E{ } denotes the *mean value*.

Further in reference to fig.4.1 we see that circuit noise current is characterised by two types of frequency

dependency. These arise from i_s and i_z which both produce constant power at all frequencies and i_f which has a 1/f power variation. We have already seen that i_z can be minimized by careful cicuit design while i_s and i_f are intrinsic active device noises uncontrollable by the system designer. Secondly the baseband signal frequencies under consideration being of the order of 1 Hz implies, in the light of the previous sections on noise, that 1/f noise may be expected to be significant. Under these circumstances, it may be assumed that i_z can be reduced by design such that it is insignificant compared to $i_x R_T/R_Z = R_T/R_Z(i_s + i_f)$. Thus we can approximate eqn.(4.12) to

$$P_N = E\{i_N^2\} \text{ , where now } i_N \cong i_x R_T/R_Z. \qquad (4.13)$$

Since i_s and i_f are both statistically independent random variables, eqn.(4.13) gives

$$P_N \cong (R_T/R_Z)^2 [E\{i_s^2\} + E\{i_f^2\}]. \qquad (4.14)$$

Now, i_s and i_f are the r.m.s. values given by eqns.(4.8) and (4.9) respectively. Thus substituting for i_s and i_f from these equations and using $\alpha=1$ and $b=2$ as previously explained, and assuming that noise is present over the whole baseband (*i.e.* $B=\partial f=f\neq 0$), we get the approximation for noise power in the current loop as

$$P_N \cong I(R_T/R_Z)^2 [2qB + KI]. \qquad (4.15)$$

We now obtain the signal-to-noise ratio (SNR) in the received current signal as I^2/P_N. This simplifies to one of two forms:

$$(SNR_o)_{CL} \cong \frac{1}{K}(R_Z/R_T)^2 \qquad \text{if } KI \gg 2qB, \qquad (4.16a)$$

and

$$(SNR_o)_{CL} \cong \frac{I}{2qB}(R_Z/R_T)^2 \qquad \text{if } KI \ll 2qB. \qquad (4.16b)$$

Fig.4.4c shows assymptotic sketches of equations (4.16) for any given value of K and B.

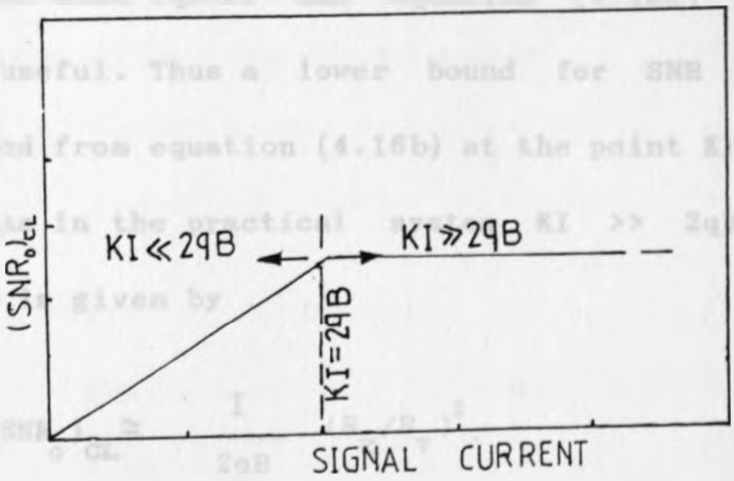


Fig. 4.4c Approximations for CL SNR.

We now make an assumption regarding the value of K. This constant satisfies $K < 10^{-8}$ for carbon microphones and bipolar transistors [10, 11]. We

assume here that K for the transmitter unit at least satisfies $K < 10^{-8}$ and since in a CL system $I(t)$ is of the order of 10^{-2} then B need only satisfy $B \ll 10^{5}$ for equation (4.16a) to be valid. Thus equation (4.16a) emerges as the more likely practical case for the monitored process for which assumption (i) in the introduction is valid.

The approximation of equation (16a) gets poorer as 2qB tends towards the value KI. A break-point is reached when 2qB=KI and equation (4.16b) becomes more useful. Thus a lower bound for SNR can be defined from equation (4.16b) at the point KI=2qB so long as in the practical system KI >> 2qB. This bound is given by

$$\min (SNR_o)_{CL} \cong \frac{I}{2qB} (R_Z/R_T)^2. \qquad (4.17)$$

Assuming that the system is matched for impedance such that $R_T = R_O + R_i$, where R_i is the resistance of the transmission line and assuming that $R_i \gg R_O$, then $R_z \cong 2R_T$ and equation (4.17) gives, in dBs,

$$\min\ (SNR_o)_{CL} \cong 191 + 10\log_{10} I - 10\log_{10} B. \qquad (4.18)$$

We note that eqn.(4.17) has been arrived at without the need to measure the value of K which can only be obtained experimentally. Eqn.(4.17) therefore avails an analytically determinable bound for the SNR in Current Loop signal transmission with easily available design parameters.

Equation (4.18) relates the CL SNR to the Loop parameters. It is seen that I improves SNR by 10 dB/decade while increase in baseband frequency degrades SNR by -10dB/decade. Thus for any situation where B and I are known, the estimate for the lower bound for SNR in the CL scheme of transmission can be obtained.

b. Comparison of CL and FM.

(i) Signal-to-Noise Power Ratio, (SNR).

For the CL system the receiver input noise current is $i_n = i_s + i_f + i_c$ where i_c is the thermal noise current associated with the resistance looking into the signal lines. SNR at the point of reception is given by I^2/i_n^2. We note however that a value I can only exist if the loop is closed. By including the receiver contribution to overall SNR we see that output SNR for the CL transmission is given by equations (4.16). For FM, we assume a transmitted signal $z(t)$ made up of a modulated carrier $s(t)$ and AWGN $n(t)$ corrupting it over the channel. Thus

$$z(t) = s(t) + n(t), \tag{4.19a}$$

$$s(t) = A_c \cos 2\pi f_i(t) \quad \text{and} \tag{4.19b}$$

$$f_i(t) = f_c + km(t), \tag{4.19c}$$

where f_c is the carrier frequency and

k is a constant.

At the receiver, bandpass filtering is assumed such that narrowband noise is present at the detector. Further, discriminator detection and a post-detection lowpass filter (LPF) of bandwidth B

are assumed. It is also assumed that on average the signal amplitude is much greater than noise amplitude $r(t)$ at the discriminator. It can then be shown [8] that above a threshold carrier-to-noise power ratio (CNR) the output SNR for FM will be given by

$$(SNR_o)_{FM} = 3\beta^2 A_c^2/2N_o B, \qquad (4.20)$$

where $\beta = \delta f/B$ the modulation index,

N_o =single-sided noise power spectral density (PSD), and

B =baseband signal bandwidth.

The said threshold is commonly taken to be 13dB and $\beta > 0.5$ [8].

(ii) A comparative criterion.

The comparison between CL and FM assumes that in the practical situation, both systems suffer equally from noise at the initial transducer conditioning. Thus comparison is limited to the noise introduced in the channel. That is, the section which the two schemes have in common.

For CL, the limiting noise is intrinsic. We assume that the thermal noise arising from the

resistance predominates over the 1/f and shot noise from the wire [11]. For FM extrinsic AWGN is predominant. The thermal noise power arising in the CL system is

$$i_o^2 = 4kTB/R_E \quad , \tag{4.21}$$

where R_E is the loop resistance looking into the transmission line from the transmitter (Fig. 4.4a).

The value of SNR over the channel is thus

$$(SNR_C)_{CL} = I^2/i_o^2 = I^2 R_E/4kTB \tag{4.22}$$

To obtain a figure of merit, M, that takes into account the noise at the transmitter, we divide equation (4.22) by this noise.

This source noise power, can be seen to be well approximated by eqn.(4.15) in the light of the foregoing discussion. M is a ratio of system SNR over the transmission channel to intrinsic transmitter noise. It thus affords a comparison between two transmission methods while taking into account source noise affecting both methods. We now find M for the CL system by

dividing eqn. (4.22) by eqn. (4.15) to get

$$M_{CL} = \frac{IR_E}{4kTB}.(R_Z/R_T)^2.\frac{1}{(2qB + KI)} \qquad (4.23)$$

$$= \frac{I}{i_o^2}.(R_Z/R_T)^2.\frac{1}{(2qB + KI)} . \qquad (4.24)$$

For an FM system the average power in the transmitted signal is $A_c^2/2$. Noise power in the message bandwidth is BN_o. SNR at output is as already stated given by equation (4.20). Define now the figure of merit for FM by dividing equation (4.20) by (4.15). Further, if the transmitter sources equal power, P_E, irrespective of whether CL or FM is used then

$$P_E = I^2R_E = A_c^2/2. \qquad (4.25)$$

Using eqns. (4.21), (4.24) and (4.25) in the figure of merit for FM gives

$$M_{FM} = M_{CL}\frac{12kT\beta^2}{N_o} \qquad (4.26)$$

The value of M in any application is greater for CL

than for FM when $N_o > 12kT\beta^2$ (4.27)

or $N_o > 4.97 \times 10^{-20}\beta^2$ at $T=300^o$ K. (4.28)

Thus whenever given β for a specific situation, the designer can use equation (4.28) to determine whether CL will be superior to FM. Equation (4.28) therefore presents a criterion for selecting between CL and FM transmission. Fig. 4.4d shows a presentation of equation (4.28) in the form of system selection regions, n_o being the normalised value $N_o/4.97 \times 10^{-20}$ at T=300 °K.

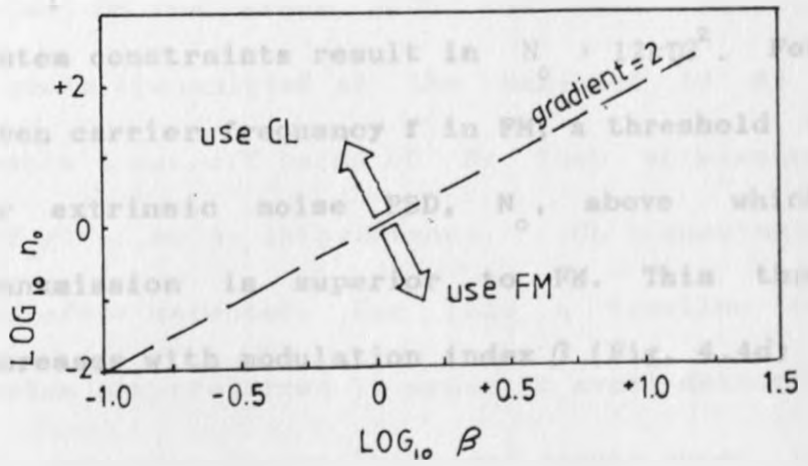


Fig. 4.4d Selection regions for CL and FM.

c. Concluding remarks on comparison between CL and FM.

An analysis of intrinsic noise effects in linear CL transmission has been presented. Figures of merit have been defined and obtained for CL and FM. A criterion, depending only on extrinsic noise PSD and the FM modulation index has been proposed for selecting between use of CL and FM. Assuming that only intrinsic noise affects CL and extrinsic AWGN affects FM transmission, then the receiver SNR in a CL system increases at +10dB/dec with signal current for constant message signal bandwidth B and fixed line impedance R_1. At fixed signal current, the SNR decreases at -10dB/dec with increase in B for fixed I and R_1. CL transmission is preferrable to FM when system constraints result in $N_o > 12kT\beta^2$. For any given carrier frequency f in FM, a threshold exists for extrinsic noise PSD, N_o, above which CL transmission is superior to FM. This threshold increases with modulation index β (Fig. 4.4d).

4.32 Practical situation at CMB.

The choice of the practical technique for front end transmission for the D.A.S. was based on the expected performance of the selected system in pertinent noise and the cost of implementation.

It will be seen from Fig. 4.3 that in fact the dominant noise coupling onto signal lines is from mains interference at 50 Hz and its harmonics. It was therefore considered that little benefit is to be derived from applying FM to the 10 Hz baseband signals. This apart from increasing circuit complexity and cost would also translate the signal in the carrier into the spectrum of the dominant noise. On the other hand low pass filtering of signals transmitted at the baseband 10 Hz would enable a cut-off below 50 Hz that eliminates the effect of mains interference. CL transmission was therefore selected. For this a baseline current system was preferred in order to avail detection of non-operative transmitters and remote power supply. It will be seen at a later point that this choice is consistent with the selection criterion of equation (4.28). The 10-50 mA standard was chosen because it

has the best SNR (eqn. 4.18) and also the largest dynamic range. This allows the system designer flexibility in introducing trade offs between system resolution and noise margin. This standard leads to higher power consumption but this was not a critical factor at all. From the foregoing it may be surmised that front-end transmission is implemented in the following steps:

- a transducer-specific signal conditioner (TT),
- a standard 10-50 mA linear current transmission irrespective of the variable monitored.

In essence therefore, if monitoring changes arise, only the design or modification of the TT units and modification of the corresponding processing programs in the receiver are required. Both of these tasks are fairly straight forward and greatly enhance the generality of the D.A.S. The TT units are not complicated and in fact can usually be purchased off-the-shelf for most types of transducers. Secondly the processing programs are structured and stored in electrically eraseable read only memory (EEPROM). Thus modifying them is straight forward.

4.4 Digital Transmission.

The main constraint governing transmission equipment design is from the channel characteristics. We shall therefore discuss the digital transmission link before attempting to specify the signal levels and data structures in Section 4.5.

In previous Sections, the electrical and physical environment has been described in detail. Measurements have shown (Fig. 4.3) that interference voltages can conceiveably go as high as 32 V r.m.s. at the ends of 100 m of a signal cable. The intuitive reaction to this fact is to consider whether running the signal cables in conduits can offer beneficial EMI shielding. Typically signal wires will run through conduits in a factory if for no other reason, physical protection. Thus any performance improvement arising from this fact may not be at increased system cost. But here we require that the conduits be metalic.

It can be shown [17] that the shielding effectiveness (SE) of a conductive barrier is given as

$$SE = R + A + B,$$

$$= 20 \log_{10} E_1/E_2 \quad \text{dB}, \qquad (4.29)$$

where

R = reflection power loss of incident field at shield boundaries,

A = absorbtion power loss of incident field in shield,

B = B-factor (dB) (neglected if A>10 dB),

E_1 = intensity of incident electric field, and

E_2 = intensity of electric field penetrating shield.

Shielding effectiveness, all other factors being constant, falls with frequency. Manassewitsch [17] shows in tables the interacting properties for various materials for which SE can be found. Assume in this case that the signal lines run in 0.5 inch iron conduit of 0.1102 inch thickness. Using these tables and corresponding design nomograms, it is found that for this shielding at 50 Hz and assuming interference by near fields only;

(i) R = 278 dB,

(ii) $A = 3.34 \times 10^{-3} t\sqrt{Gf\mu}$ dB,

where t = thickness of shield in mils,

f = frequency of incident field,

μ = relative permeability of shield referred to free space, and

G = relative conductivity of shield referred to copper.

Substituting then for G=0.17, t=1102, μ=1000 and f=50, we find $A \cong 50$ dB. We thus ignore B as stated above and apply equation (4.29) to find, SE = 328 dB.

(iii) It is seen from Fig. 4.3 that noise pick-up levels introduce voltages of up to 0.32 and 0.07 V/m common and differentially measured interference respectively without shielding.

Assuming that a measurement system will use differential mode measurement across a pair of signal lines, we then let E_1 = 0.07 V/m. Applying equation (4.29) and substituting for SE we find that the field actually penetrating the conduit is $E_2 = 2.8 \times 10^{-18}$ V/m.

This is equivalent to 2.8×10^{-16} V/100m.

(iv) If simplicity and cost of circuitry requires that the digital link be within the range of TTL logic then the nominal transmission voltage is 5V. This achieves a signal to noise ratio (SNR) for 100 m range of 325 dB. (By dividing the signal power with noise power found in 4.4(iii)). If no shielding is used, and random TTL data is assumed (*i.e.* a data r.m.s. value of 2.5 V), the SNR at the 100 m range would be -9 dB. Either case assumes baseband transmission.

It is clear that if shielding is used, the SNR at the receiver is so high as to imply no need for its improvement by further signal processing at the transmitter. This suggests that no carrier modulation is called for in the digital link on account of continuous noise discussed so far. We now look briefly at impulse noise.

It was seen above that shielding affords an attenuation of 328 dB for electromagnetically coupled interference. Consequently the possibility of radiated impulse noise corrupting the data through this path is remote. However it remains of interest because the

proposed D.A.S. need not be unnecessarilly constrained to use wire pair digital transmission. The possibility of using a radio link instead will completely change the treatment of the problem of noise. Thus though a carrier modulation system was not implemented it is nevertheless mentioned for the sake of completeness.

Use of radiolink for digital transmission necessarily implies use of a carrier system. Of the digital modulation methods, it has been shown [8, 14] that coherent phase shift keying (PSK) has the lowest probability of error, P_e in additive white Gaussian noise (AWGN). Engel [18] has also shown that this is also true in impulse noise. However coherent signaling is difficult to implement in practise and a non-coherent technique though inferior in noise performance may be preferable. Among such techniques, differentially coherent PSK (DPSK) has the lowest P_e [18]. It is also simple to implement, especially at the transmitter. It would therefore be the recommended carrier system for the D.A.S. An enlightening evaluation of this method and its comparison with other common methods is detailed in

[18].

In this Section transmission at the rear end has been discussed. The convenience of easily ensuring a very high SNR at the receiver has been cited in favour of using digital baseband transmission. It has been implicitly assumed that the requisite data transmission rates are possible within this SNR margin without need for modulation. This is especially so because SNR degrades as the bit duration of digital data decreases [19]. However as was previously mentioned, power considerations are not critical here and if a need arises it is straight forward to adjust the average power per symbol upwards. Hence baseband transmission was preferred at the rear end.

In the next section we look at the properties of the signals and data flowing through the D.A.S.

4.5 Signal Descriptions.

In this section details of all the signals passing through the D.A.S. are expounded . An integrated view

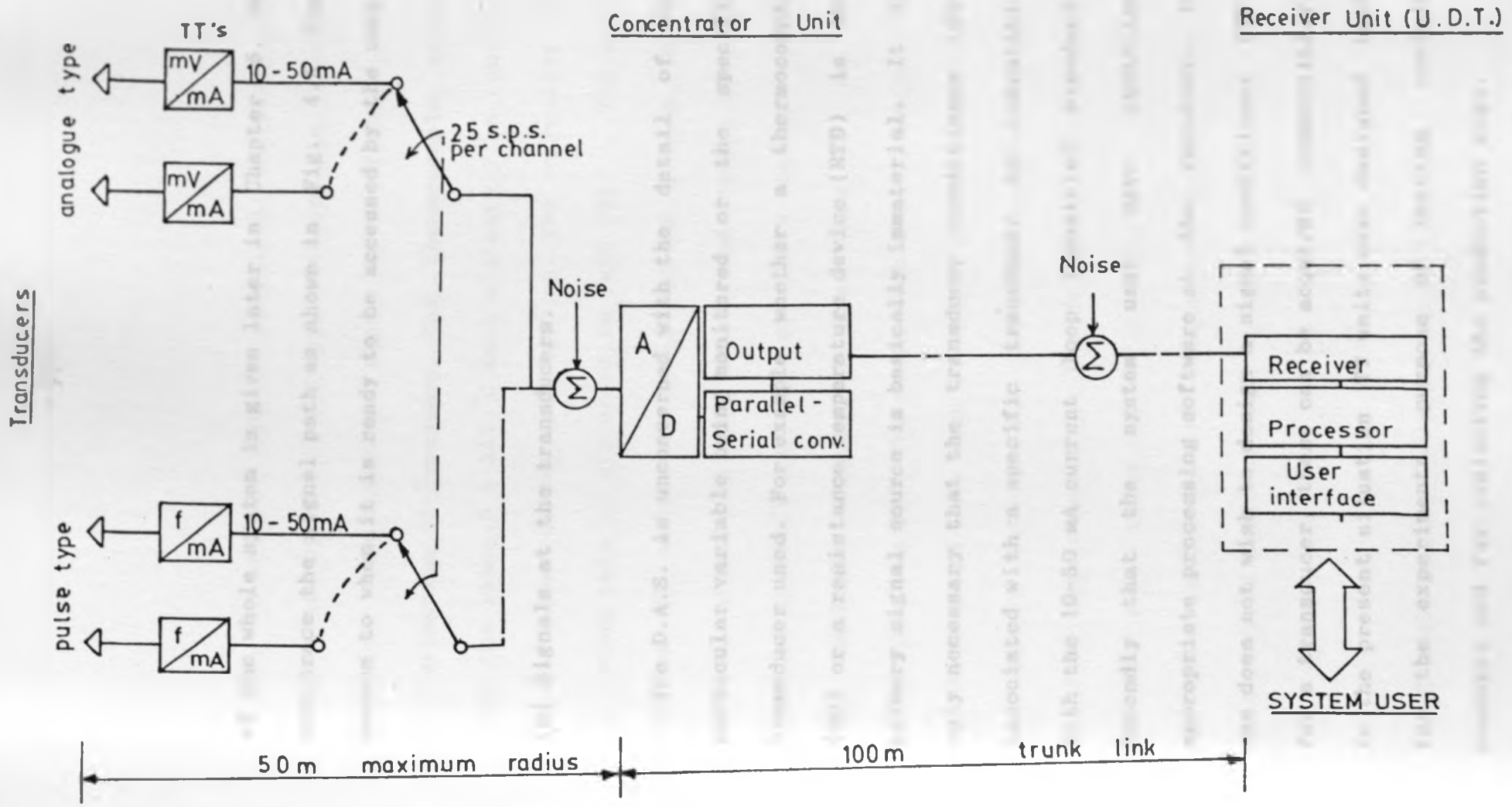


Fig. 4.5 Conceptual model of the D.A.S.

of the whole system is given later in Chapter 5. We now trace the signal path as shown in Fig. 4.5 from source to when it is ready to be accessed by the user.

(a) Signals at the transducers.

The D.A.S. is unconcerned with the detail of the particular variable being monitored or the specific transducer used. For example whether a thermocouple (TC) or a resistance temperature device (RTD) is the primary signal source is basically immaterial. It is only necessary that the transducer conditioner (TT) associated with a specific transducer be compatible with the 10-50 mA current loop industrial standard. Secondly that the system user have installed appropriate processing software at the receiver. If one does not wish to design a signal conditioner (TT) for a transducer, these can be acquired commercially. In the present situation TT units were designed both for the experimental purpose of testing certain concepts and for evaluating the production cost.

Two types of functions were required of the TT

units. The analogue type is required to sense oven temperature by use of a K-type thermocouple. Then cold junction compensation must be effected and linearisation if necessary. The thermocouple voltage over the range 0 - 250 $^{\circ}$C must ultimately be converted into a linear current of 10-50 mA. The circuitry for achieving this is discussed in Part III. The second type of TT units convert counting pulses into a current signal in the front end loop. They are required to condition the proximity sensor outputs into analogue signals of less than 10 Hz. In particular the TT's for ovens should be optimized for counting rates less than 1.7 per s and tuned for best performance between 0.9 and 1.3 counts per s. Critical requirements for the design of the analogue (TT-A) and pulse (TT-P)conditioner units are robustness and small size. The actual designs used in this project are discussed in Part III.

(b) Signals at the Concentrator Unit;(C.U.).

(i) Input Setup.

The C.U. has to perform the task of loading all the information arriving via the various current loops onto the single digital link to the receiver. It was shown in Table 2.1 that a total of at least 42 channels are expected to be served. Each of these was shown to have at most a bandwidth of 10 Hz. The protocol for signal handling at the C.U. was kept to the simplest possible - analogue signal multiplexing then analogue-to-digital (A/D) conversion and finally serial data transmission. We now consider signal sampling and quantization.

(ii) Sampling.

A design criterion has already been established limiting the maximum baseband signal to 10 Hz. Low pass filtering with cut-off at 10 Hz is therefore desirable at the sampler inputs. Nyquist's Sampling Theorem [14] shows that such a signal can be sampled and completely reconstructed if the sampling rate is equal to or greater than 20 samples per second (s.p.s.). Practical constraints on the design of reconstruction filters result in sampling rates exceeding Nyquist's value; usually by about 20% in the

case of telephone systems [20]. Applying a 25% excess to the D.A.S. gives a sampling rate of 25 s.p.s. allowing for a reconstruction filter roll-off of 5 Hz. Although no requirement exists in the present system for analogue outputs requiring such reconstruction , a future need can thus be accommodated. (Betts [21] gives a very useful treatment of an approximate method for the specification of the required anti-aliasing (reconstruction) filters).

The second point arising at the sampler regards the duration of the sampling pulse. Nyquist's Theorem assumes impulse sampling which is not possible in practice as a sampling pulse must be of finite duration because of the A/D action. Sampling pulses of finite width give rise to different effects in the sampled spectrum depending on the shape of the sampled pulse. In "natural" sampling the sampled signal is allowed to change during the sampling duration *i.e.* while A/D conversion is taking place. "In flat-top" sampling the level of the sampled signal is held ("frozen") during the sampling duration - that is an instantaneous sample is taken but prolonged until A/D

conversion is complete.

It can be shown [14] that "natural" sampling only has an attenuating effect on the reconstructed waveform. It is therefore not complicated to use as D/A reconstruction will require only filtering and linear amplification. However for accurate A/D conversion, natural sampling is only possible with fast A/D coverters and practicable only for fairly low input signal frequencies. On the other hand flat-top sampling while more versatile, introduces both amplitude distortion and a time delay into the reconstructed signal [14]. This is called the "aperture effect". This distortion is related to the duty cycle of the sampling pulse *i.e.* the ratio of the duration by which the sampling impulse is prolonged, to the sampling period. Since the distortion is non-uniform and frequency dependent, it can only be removed by equalization circuitry in the reconstruction process. However, it can be shown [14] that for sampling duty cycle of 10% or less the amplitude distortion arising because of flat-top sampling is less than 0.4%. It follows then that correction for this effect would be unnecessary.

We now apply the results of the above discussion to the D.A.S. It is clear that sample-and-hold (flat-top) sampling should be used because otherwise a fast and expensive A/D converter would be required. Further, such a converter would offer little flexibility if D.A.S. A/D conversion requirements were to change in future. The sampling rate is 25 s.p.s. for a total of 48 channels. Hence the sampling clock must run at 1200 Hz or a period of 833.3 μs. Suppose it is decided that reconstructed signals are to need no correction for distortion introduced by sample-and-hold conversion; then a 10% duty cycle for the converter gives a maximum A/D conversion time of 83.3 μs. Further, if such an A/D converter uses a counter technique and N-level quantization, then the counter must be clocked at at least 83.3/N μs. However these strictures need be applied only where reconstruction of the sampled signal to analogue form is desired under the conditions stated above.

(iii) Quantization.

It is desirable that temperature data be resolvable to at least 1 $^{\circ}$C over the range 0-250 $^{\circ}$C.

Thus a 256 level binary quantization is just adequate. This produces 8-bit words for each A/D conversion. It also requires that the receiver part of the C.U. be able to resolve current levels in the loop to at least 0.16 mA.

For the counting channels the minimum number of quantization levels is equal to the maximum required counts/s capability if a resolution of one count is desired. It is seen that for low count rates 8-bit words will not be necessary. In this case certain bits may be added to the count data to complete an 8-bit word with extra bits used for data protocol implementation or error control at the receiver. However the use of non-uniform data word lengths complicates both transmitter and receiver design. Thus although it may be used at a later date the capacity for non-uniform data word length is not explored here. All the signals reaching the C.U. are converted into 8-bit data words. The signal-to-quantization-noise ratio (SNR) is given by [8]

$$SNR_Q = \frac{12I^2}{d^2} \qquad (4.30)$$

where I is the r.m.s. value of the signal current,

and d is the quantization step.

Thus for CL transmission, the lowest signal level in the 10-50 mA standard is 10 mA. Using 256 level quantization gives d=0.16 mA; similarly for counting channels. Thus applying equation (4.30), the minimum value of quantization SNR is given by

$$\min (SNR)_Q = 47 \text{ dB}$$

We note that uniform quantization has been used. The consequence is that a better SNR_Q is obtained for high values of signal input than for the low levels. For both the temperature and counting signals this is in fact desirable. The reason is that normal production runs operate at the higher end of the D.A.S. monitoring range. Hence any process giving rise to better system performance at that end is desirable. It is also worthwhile to note that 8-bit quantization gives excessively high resolution for the counting channels reading 1.7 counts/s (c.p.s). However counting tasks at CMB are widely varied from the very slow (ovens at 1.7 c.p.s.) to the fast (canlines at 13 c.p.s.) to the very fast (presses in excess of 1000 c.p.s.). Thus it is more logical to reconfigure the

application software to deal with the desired resolution than to limit channel resolution in hardware design.

(c) Digital Link Transmission Protocol.

The 48 channels each of 10 Hz are sampled at 1200 Hz and 8-bit A/D conversion performed. This produces a serial data output rate of 9600 bits per second (b.p.s.). In the following discussion we will try to analyse the characteristics of the transmission of this data to the receiver. In particular the decision to transmit it in baseband over a wire channel has already been explained in Section 4.4. Some of the outstanding issues include the formatting of the transmitted serial data, link limitations, expected data error rate and link reliability.

(i) Data format.

The choice of a standard 8-bit word has already been explained. For reasons of simplifying implementations, it is desirable that an easy framing format be used especially if the front end is not "intelligent" *i.e.* microprocessor controlled. This is

because all data formatting then requires hard wired implementations. It was therefore chosen that data be formatted in form of frames, one frame consisting of a single sample from each channel. Hence a frame contains 48 data samples and 384 data bits. Further a framing pattern 8-bits long is used to separate frames. Consequently channel 0 was selected as the framing channel leaving 47 channels for input signals. This arrangement makes it easier to recover the frame and the data bits in it at the receiver so long as the bits themselves are synchronised. It will be explained in Part III how this enables clocks on the transmitter and receiver to be synchronised. The cost of this framing arrangement in terms of link performance will be discussed shortly.

(ii) Channel bandwidth considerations.

It is known [14] that the transmission bandwidth of a pulse is about twice the reciprocal of its duration. Thus a bit rate of 9600 requires a transmission bandwidth of about 20 KHz. We can model a wire pair as a resistor, R and capacitor, C (RC) low-pass filter. This is possible since the frequencies under

consideration as already mentioned fall below 250 kHz. It can be easily shown that the 3 dB cut-off frequency for this filter is given by

$$f_{3dB} = 1/ 2 \pi R C.$$

Hence by knowing the input impedance of the receiver and the primary characteristics of the wire an appropriate wire type can be chosen to meet the bandwidth requirements for the digital transmission.

Suppose now a wire size of 24 a.w.g. (0.53 mm diameter) is chosen for the link. This has a capacitance C = 5.2 nF and resistance R = 15.5 ohm for a loop length of 100 m [22]. Its 3 dB frequency is thus equal to about 2 MHz. Thus a 20 KHz signal travelling along it experiences virtually no distortion. We therefore disregard the issue of intersymbol interference in this case. The same wire has a characteristic impedance $Z \cong 181\angle -33.3$, attenuation of about 0.5 dB/100 m and phase shift of 3.9°/100m . It is clear that even with load matching to eliminate signal reflections this argument remains valid.

(iii) Probability of bit error.

Consider that it has been stated that baseband logic levels are transmitted in the digital link. Assume first that no specific logic level has been selected among the possible such as TTL, ECL or CMOS. Let us thus suppose a general receiver logic which interprets a signal to be LOW if it is equal or below V_{IL} and HIGH if it is above or equal to V_{IH}. Suppose the data from the transmitter has the logic levels V_L and V_H for LOW and HIGH respectively. The data arriving at the receiver is superimposed with both noise and intersymbol interference (II). But we have already shown that II can be ignored and that the noise may be treated as zero mean additive and white (AWGN). It can be shown that the probability destribution function (pdf) of white noise of mean m and variance σ^2 is given by [15]

$$p(n) = \frac{1}{\sqrt{2\pi\sigma^2}} \exp\left[-(n-m)^2 / 2\sigma^2\right]. \qquad (4.31)$$

In general, digital systems, have LOW = V_L as approximately zero volts although HIGH may vary. We therefore assume for simplicity and directness that V_L=0. The pdf's of the received data are shown in Fig. 4.6

for LOW and HIGH transmission.

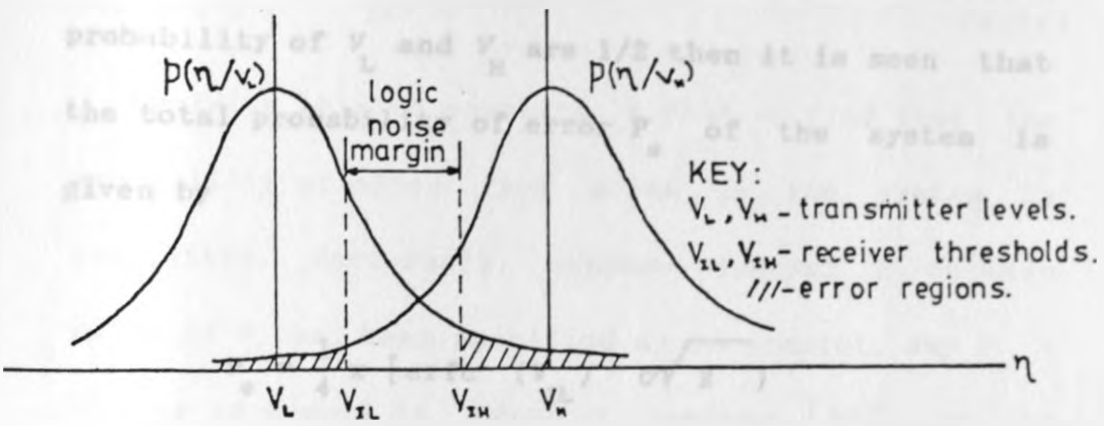


Fig. 4.6 Conditional probability density functions at the digital receiver.

There are two ways in which transmission bit errors occur. If V_L is transmitted, an error occurs if the received voltage $V_r \geq V_H$ the threshold voltage for HIGH. The probability of this event as seen from Fig. 4.6 is given by 1/4 erfc($V_{IH}/\sigma\sqrt{2}$) where erfc(x) is the complimentary error function defined as 1-erf(x) and

$$\text{erf}(y) = 2/\sqrt{\pi} \int_0^y e^{-x^2} dx. \qquad (4.32)$$

Similarly an error occurs if V_H is transmitted and $V_r \leq$

V_{IL} is received. The probability of this happening can similarly be seen to be 1/4 erfc($V_{IL}/\sigma\sqrt{2}$). If the data transmitted is random such that the *a priori* probability of V_L and V_H are 1/2 then it is seen that the total probability of error P_e of the system is given by

$$P_e = \frac{1}{4} \times [\text{erfc}\ (V_{IL}/\ \sigma\sqrt{2}\ ) + \text{erfc}\ (V_{IH}/\sigma\sqrt{2}\ )] \qquad (4.33a)$$

For the HCPL 2601 high speed opto-isolator device used on the D.A.S. receiver, V_{IL} = 0.8 V and V_{IH} = 2.0 V. It is known from signal processing theory [15], the noise quantity σ^2 represents its power and hence σ is its r.m.s. voltage. The noise voltage coupling onto the signal lines was found in Section 4.4 to be σ = 2.8 x 10^{-16} V at the receiver.

Applying the data above to equation (4.33a) gives

$$P_e = \frac{1}{4} [\text{erfc}\ (2.0 \times 10^{15}) + \text{erfc}\ (5 \times 10^{15})] \qquad (4.33b)$$

Haykin [14] shows that when the argument of the error function is much greater than unity,

$$\text{erfc}\,(x) \cong e^{-x^2} / (x\sqrt{\pi}) \qquad (4.34)$$

Applying this to equation (4.33b) we find that the probability of error from noise in the system is negligible. Conversely, suppose instead a certain value of P_e had been specified as the target, say $P_e = 10^{-6}$ as is common in computer systems [19]. It is possible by use of equation (4.33a) to calculate the maximum noise level acceptable on signal lines. A situation like this can arise if for example it is desired to investigate the use of alternative signal shielding techniques or logic levels.

(iv) Framing performance.

The ability to correctly receive the transmitted bits is a necessary but not sufficient condition for successful transmission. In order for received data to be interpreted properly at the receiver the original relationships between the various bits must be restored. In this case for example the receiver must be able to form 8-bit words as they were before serial transmission. The congruency of the 48 channels

must also be restored. We investigate here the performance of a system with a bit error probability P_e.

Suppose the frames are L bits long. Consider a framing scheme in which a single bit error in the framing pattern gives rise to a framing error. Let n be the number of bits in the framing pattern itself. The probability of a framing error P_f is [8],

$$P_f \cong nP_e. \tag{4.35}$$

Suppose a loss of frame is declared by the receiver if k failed attempts are made to capture the frame pattern. The probability of a loss being declared (framing failure) is

$$P_l \cong (nP_e)^k. \tag{4.36}$$

If F frames are transmitted per second, the average time between frame losses in seconds is given by

$$T_l \cong (nP_e)^k/F. \tag{4.37}$$

Let now a frame be considered re-acquired when the framing pattern appears m times in the same position. (This ensures that a random n-bit pattern is not mistaken for the framing pattern). It can be shown [8]

that the average worst case time required to detect a frame loss and re-acquire is

$$T = k + m + L/(2^n - 1) + 1 \quad \text{frames.} \qquad (4.38)$$

For the D.A.S. these parameters are seen to be; n=8, L=384 and F=1200 while k and m are software configurable. (These latter values are defaulted to unity in the D.A.S.). If P_e is known for a given link these values can be calculated to give an indication of its performance.

In this chapter the details of the signals passing through the D.A.S. have been exposed. An attempt has been made to illuminate the key points related to system performance. The treatment has assumed that the action at the receiver will not affect system performance in terms of actual signal processing. As far as the recovery of the signals in noise is concerned this is justifiable if the receiver unit is treated as the end user. In fact this is the case in the D.A.S. as will be clear after the description of the physical implementation. In the next chapter will be given the D.A.S. specification summary after which

Part III will deal with the practical issues of the actual D.A.S. implementation and performance.

CHAPTER 5

SYSTEM SPECIFICATIONS SUMMARY

This chapter summarises the most important points raised throughout Part II. In it are given brief functional specification guides for each of the prototype modules designed in this project. It is later shown that these modules worked satisfactorily and can be used as prototypes.

5.1 Hardware Specification Summary.

5.11 Transducer transmitters.

The design of a TT will depend on the expected input signal. Thus a unit for temperature (TT-A) will be different from that for counting (TT-P). However all TT's output are standard linear 10-50 mA currents. For the D.A.S. two types of TT's were initialy designed. These units operate in a severe environment, especially with respect to temperature and harmful ingression of soot and dampness.

a. Temperature type: TT-A.

The functions of this unit are to:

(i) extract, sense and amplify thermocouple signal,

(ii) apply cold junction compensation,

(iii) linearize thermocouple signal if necessary,

(iv) convert 0-250 ^{o}C temperature range to 10-50 mA current and

(v) interface signal current to loop current.

The basic specifications of this unit are:

Input bandwidth: 10 Hz.

Supply current: 10 mA ±1%.

Input signal range: 0-20 mV.

Output signal range: 10-50 mA.

Overall accuracy: 1%.

Operating temperature: 70 ^{o}C max.

Ingress protection: IP 66.

b. Pulse type: TT-P.

The functions of this type of transducer transmitter are to:

(i) convert count sensor output voltage pulses into 10-50 mA signal current and

(ii) interface the analogue current signal into the Current Loop.

The basic specifications of this type of unit are:

Input pulse rate: 20 counts/s.

Output bandwidth: 10 Hz.

Supply current: 10 mA ±1%.

Output signal range: 10-50 mA.

Overall accuracy: 1%.

Operating temperature: 70 °C max.

Ingress protection: IP 66.

5.12 Current Loop transmission.

The 10-50 mA current loop analogue baseband transmission technique is the standard link between each TT and the Concentrator Unit. The Loop is designed to the following basic specification:

Loop length: 100 m.

Loop medium: 24 a.w.g. copper wire pvc insulated.

Current rating: 1 A.

Input impedance: 15.5 Ω.

Protection: Mechanical damage.

5.13 Concentrator Unit.

This unit collects together all the information arriving over the CL links. This information is processed in the C.U. and then forwarded over a single

digital link. In particular, the C.U. performs the following tasks:

(i) multiplex current loop channels to a current detector/receiver,

(ii) sample the signals from each analogue channel and perform A/D conversion,

(iii) append a framing pattern to the data,

(iv) convert framed data to bit-serial format and

(v) interface serial data train to twisted wire pair digital transmission link.

The basic specifications of the C.U. are:

Input signal range: 10-50 mA.

Sensitivity/Resolution: 10/0.16 mA. min.

Comparator hysteresis: 50 mV.

Input signal bandwidth per channel: 10 Hz.

Number of input channels: 48.

Sampling rate: 25 samples/channel/s.

A/D conversion period/hold time: 833/83.3 μs.

Quantizer reference: 2.5 V.

Quantization levels: 256/8-bit.

Quantization SNR: 47 dB.

Output mode: Digital TTL.

Power supply: 36 W.

Ingress Protection: IP 51.

5.14 Digital link.

Transmission from the C.U. takes place in baseband over a digital twisted-pair trunk link. This goes over about 100 m in a high electrical activity area in which noise pick-up has been measured to reach as high as 7V r.m.s. Predominant noise is at the 50Hz line frequency but presence of higher frequencies is also indicated. The design and performance expectations for this link are as follows:

Length: 100 m.

Medium: 24 a.w.g. copper wire twisted-pair 52pF/m.

Channel SNR: 328 dB (with link in metalic conduit).

-9 dB (unshielded).

Data rate: 9600 bits/s.

Link characteristic impedance: 181∠-33.3.

Signal attenuation over 100 m: 0.5 dB at 20 kHz.

Signal phase delay over 100 m:3.9°.

Framing efficiency: 98%.

Expected P_e : 0 (nominally if shielding is effective).

5.15 User-end Data Terminal.

This unit performs the role of D.A.S. output. It interfaces the D.A.S. to the user. To do this it must link successfuly with the C.U., perform a certain amount of data processing and respond to at least a minimal set of operator inputs. In particular, the U.D.T. performs the following functions:

(i) receive and reframe arriving data,

(ii) assign and append source information onto arriving data,

(iii) append real-time information onto the data,

(iv) accept operator inputs to the D.A.S. and execute accordingly,

(v) format information for output filing and

(vi) interface the D.A.S. to output devices *e.g.* RS 232C bus.

The following are the basic specifications of the U.D.T.:

Inputs: Serial TTL data 9600 bits/s.

Operator enabled buffer to U.D.T. data bus.

Microprocessor: Z80 2.5 MHz.

Memory: ROM;EEPROM 2K,

RAM: 2K,

Reserve 4K.

Software: Basic firmware operating system, expandable.

Output: Serial RS 232C standard. UART 300/600 bits/s.

PART III

System Implementation

This Part of the report elaborates on the implementation of the D.A.S. discussed in Parts I and II. In it prototype circuit designs are proposed and their performance in tests described. This Part closes with sections on Recommendations, Conclusion and a discussion on areas of Further Work.

Chapter 6 covers in qualitative detail the implementation and functioning of the hardware. Chapter 7 is devoted to D.A.S. software. Chapter 8 is the concluding chapter including aspects of System integration and the closing remarks.

CHAPTER 6

HARDWARE IMPLEMENTATION

A realization of the D.A.S. described and analysed in the previous two Parts is presented in Chapters 6, 7 and 8. It is stressed that this particular hardware implementation as a solution to the data acquisition problem is itself not general but rather, efficient in the sense of achieving a unique set of original objectives. Alternative approaches to this hardware realization are indeed conceivable. For example, instead of designing a system as the one that follows here, add-on boards (available on the electronics market) could be used with a personal computer (PC) [23, 24, 25]. Or a basic data acquisition unit such as a Data Logger could have been purchased and a system designed around it. The devices and techniques applied in the hardware here could have been different but aim at the same performance level. Nevertheless what appeared the best solution was chosen.

The reasons for the particular approach used here have been justified in previous discussions. But an attempt is made to clarify them wherever possible in

the following texts of the circuits' descriptions. An acknowledgement is however made that there are always ways of doing things that are out of the designer's personal preference rather than pure technical reason. Thus although the most systematic and logical way is intended here, signs of this bias may still be evident in the circuits. So long as the intended functions are clear there aught to be no harm in that. With that, a designer wishing to work on a production version of the D.A.S. is at liberty to exercise his own discretion. In describing the following circuits we will therefore concentrate on functions and how they are achieved here rather than alternative methods. This Chapter should be read with Section 5.1 in mind.

6.1 Transducer Transmitters (TT's).

These are the units that condition the variable being monitored to interface to the D.A.S. The inputs of the TT's are the transducer outputs. The outputs of the TT's are a standard 10-50 mA current linearly varying with the input signal. For each kind of variable to be monitored an appropriate TT is required. Two types of these units were designed in

this case. TT-A units were used to interface a thermocouple input and TT-P were used with proximity sensor counters.

A circuit diagram of a TT-A unit is shown in Fig. 6.1. The function of the circuit is to convert the millivolt input from a thermocouple (TC) into a linear 10-50 mA current.

The heart of the unit is the AD595AQ thermocouple amplifier. This IC is used to preamplify the TC input, perform cold junction (ice-point) compensation, linearize and amplify the signal to give a 10mV/$^{\circ}$C output. It can do this for J or K type TC's. The variable resistors attached to the AD595AQ are used to tune it to specific applications outlined in the manufacturer's (Analog Devices Corp.) data sheet. IC 2 and Q1 are used to convert the output of IC 1 into a current through R5. The circuit is calibrated with a thermocouple simulator for the voltage output at TP1. The signal dependent value of the loop current is given by $V_{TP1}/R5$. R5 is adjusted such that the current in the loop is set to the required lower limit such as 10mA. The network of IC 2 and Q1 has a unity transfer function between TP1 and TP2. D1 goes "ON" when the TC

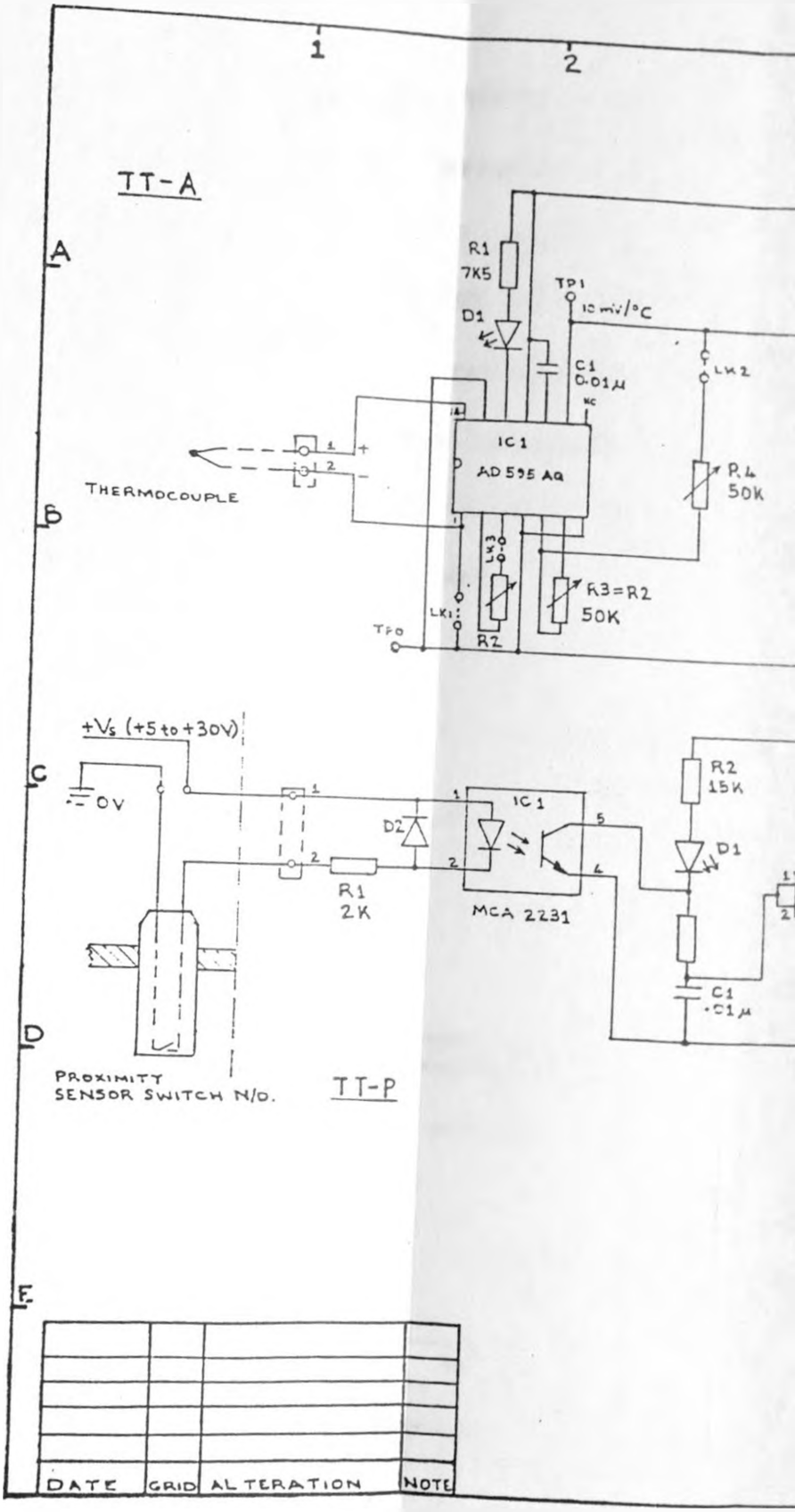
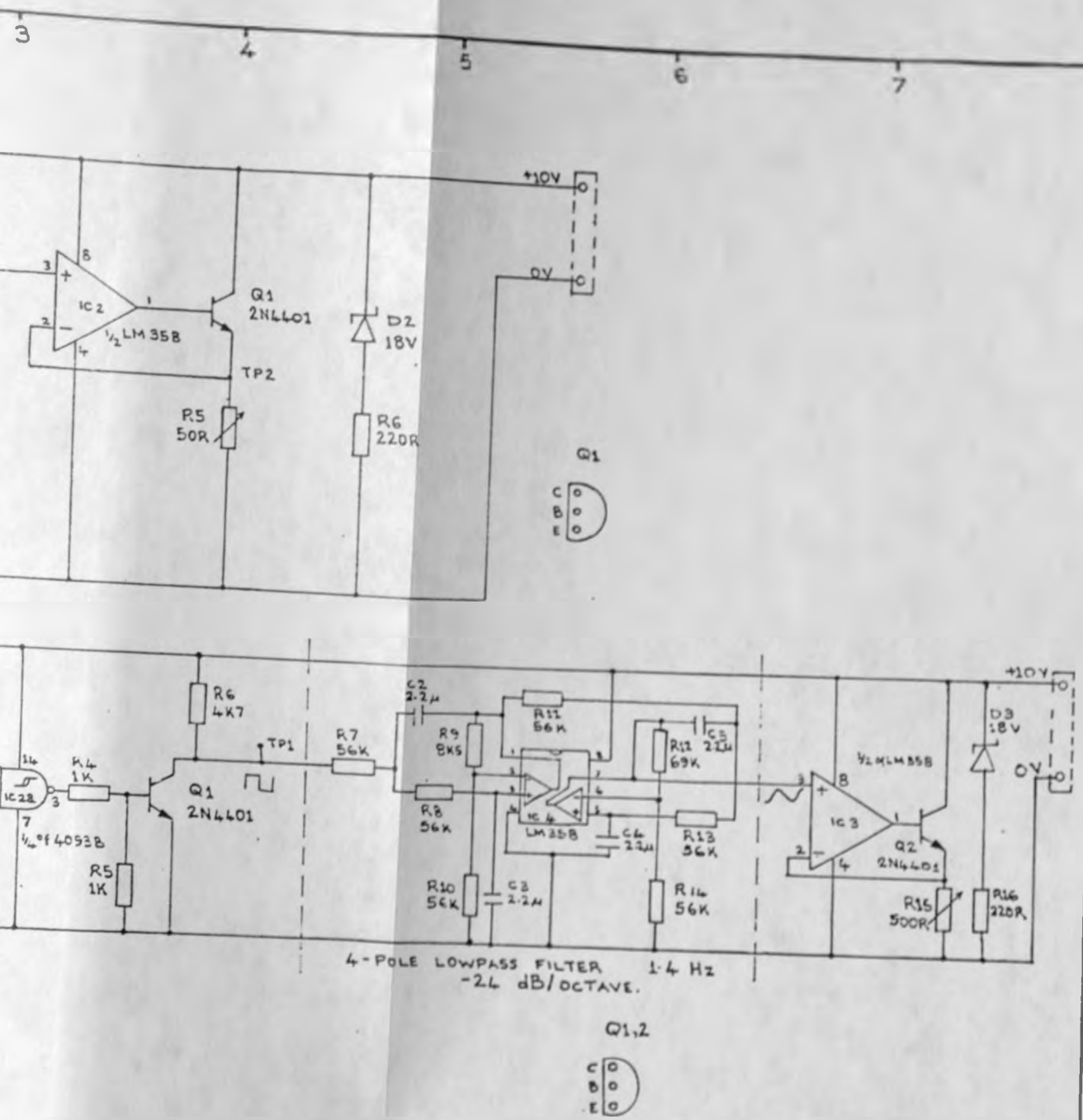

1
2
TT-A
A
B
C
D
E
R1
7K5
D1
TP1
10 mV/°C
C1
0.01μ
LK2
IC1
AD 595 AQ
P.4
50K
THERMOCOUPLE
LK1
TP0
R2
R3=R2
50K
+Vs (+5 to +30V)
0V
D2
R1
2K
IC1
MCA 2231
R2
15K
D1
C1
·01μ
PROXIMITY
SENSOR SWITCH N/O.
TT-P
DATE
GRID
ALTERATION
NOTE

Fig. 6.1



TITLE: SCHEMATIC DRGS FOR TT UNITS	
	SHEET 1 OF 1
PART: DAS-01/02 PASSY DRGS	DEMO1
ORIGIN: Dept of E.S.E. Eng., University of Waikato.	DATE: NOV 1988. ©

Circuit diagrams for the TT units.

is open or otherwise overloading the AD595. D2 protects the networks connected to the current loop from steady or surge over-voltage. Fig. 6.2 shows a curve obtained for temperatures from 0 to 250 ^{o}C with a TC simulator used at CMB, Thika. A recommended calibration procedure is given in the Section, "Commissioning Notes" in Chapter 8. Similarly also a discussion on performance of this TT-A circuit.

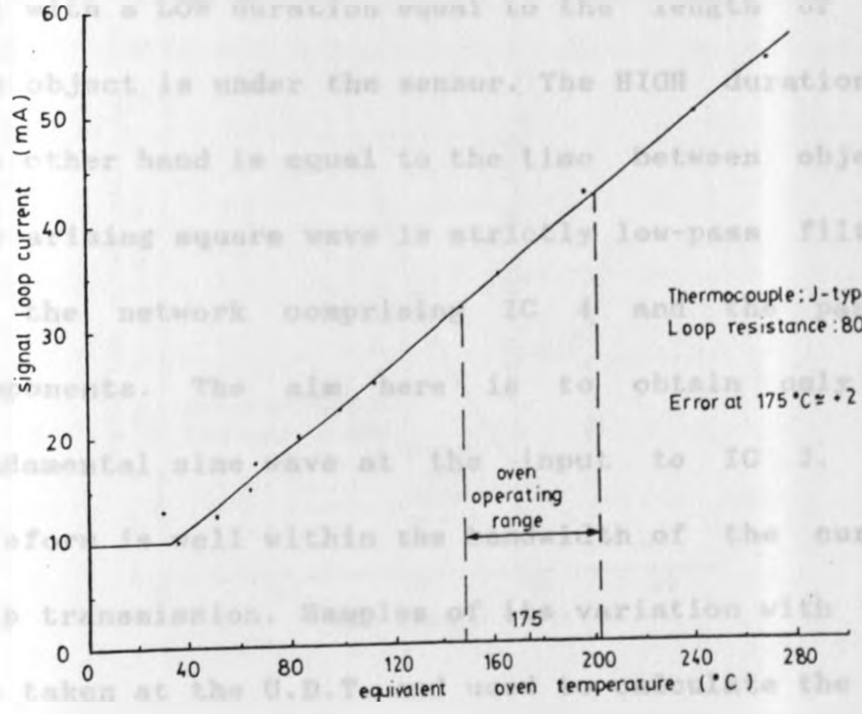


Fig. 6.2 Temperature to current conversion by the TT-A.

The counting type of unit, TT-P was realised using the circuit diagram of Fig. 6.1. The connection of the counting transducer is shown on the extreme left. The MCA2231 opto-isolator is used because sensor voltages are widely varied and generally isolation is needed. When the sensor head closes its switch, the MCA 2231 shorts to ground D1 and discharge C1. D1 lights up to indicate sensing and IC 2a grounds point TP1. When the sensed object moves out of the range of the sensor head, TP1 goes high. Thus a square wave is produced at TP1 with a LOW duration equal to the length of time the object is under the sensor. The HIGH duration on the other hand is equal to the time between objects. The arising square wave is strictly low-pass filtered in the network comprising IC 4 and the passive components. The aim here is to obtain only the fundamental sine wave at the input to IC 3. This waveform is well within the bandwidth of the current loop transmission. Samples of its variation with time are taken at the U.D.T. and used to calculate the time between peaks (*i.e.* reciprocal of its frequency). [Alternatively the amplitude of the waveform can be used to convey information on counting rate as

described in Section 8.1 (ii)]. From this the units passing the sensor head every second can be worked out. IC 3 and D3 perform the same task as those described for the TT-A. Fig. 6.3 shows the basic transfer characteristic of this circuit. The limitations as well as the theoretical techniques used for this circuit are deferred for analytical detail to the write up on Commissioning.

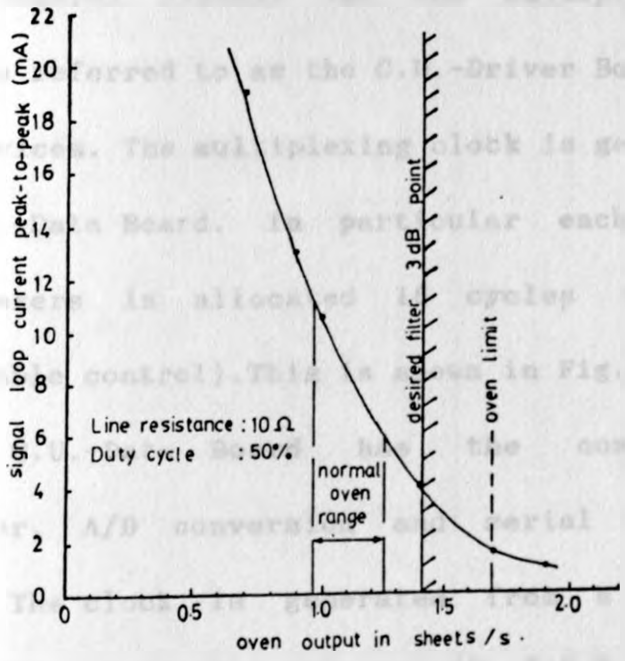


Fig. 6.3 TT-P characteristic.

6.2 Concentrator Unit (C.U.).

The Concentrator Unit performs the function of multiplexing the samples from the 48 current loop channels, A/D conversion and digital transmission. It was constructed on two separate boards; one analogue and the other digital. These are shown in Figs. 6.4 and 6.5. The analogue board holds 3x16 channel analogue multiplexers together with the channel input connector and RC low pass filters. On this board also is the control circuit for the multiplexing. This board is referred to as the C.U.-Driver Board and uses CMOS devices. The multiplexing clock is generated from the C.U.-Data Board. In particular each of the 3 multiplexers is allocated 16 cycles of MUX 0 (MUX-enable control).This is shown in Fig.6.6.

The C.U.-Data Board has the control clock generator, A/D conversion and serial transmitter driver. The clock is generated from a crystal at 2.4576 MHz and divided down by IC 7,8,9 and 10 to perform various functions. R1 and R4 are used to vary the level of the signal reaching IC 1 and are used for calibrating the framing pattern. IC 1 is a buffer for the analogue comparator. The network of IC 2,3 and 4

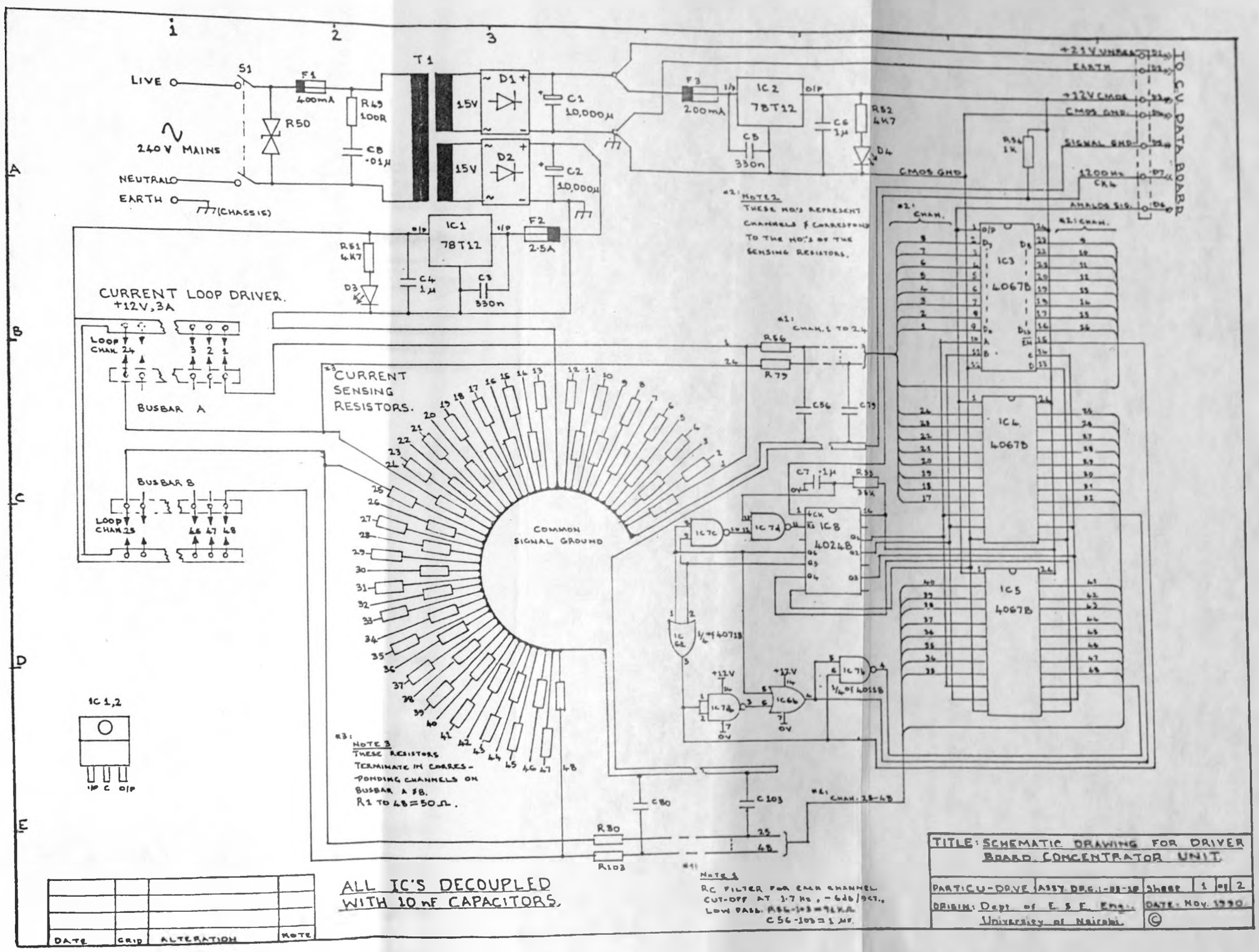


Fig. 6.4 Circuit diagram of the C.U.- Driver Board.

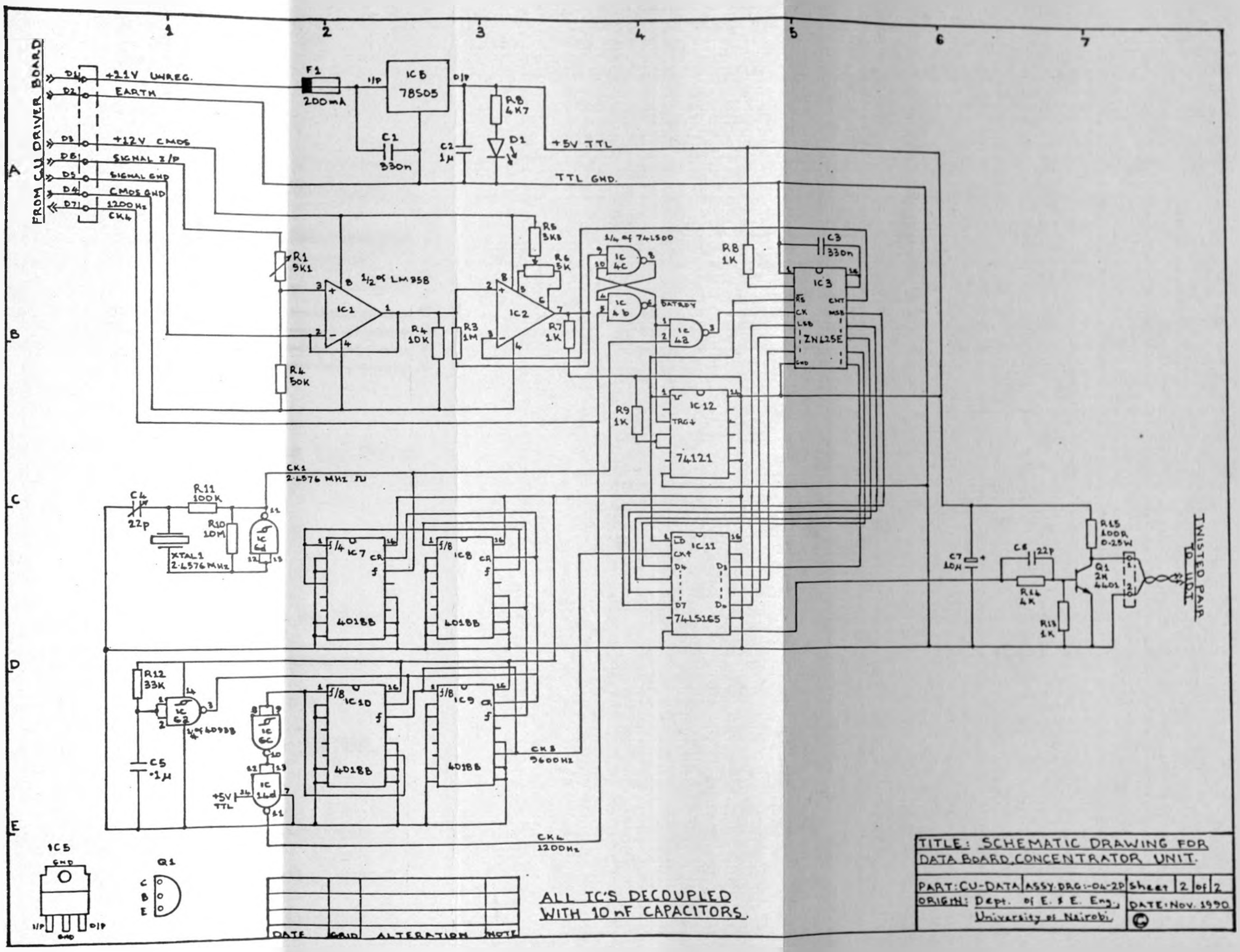


Fig. 6.5 Circuit diagram of the C.U.-Data Board.

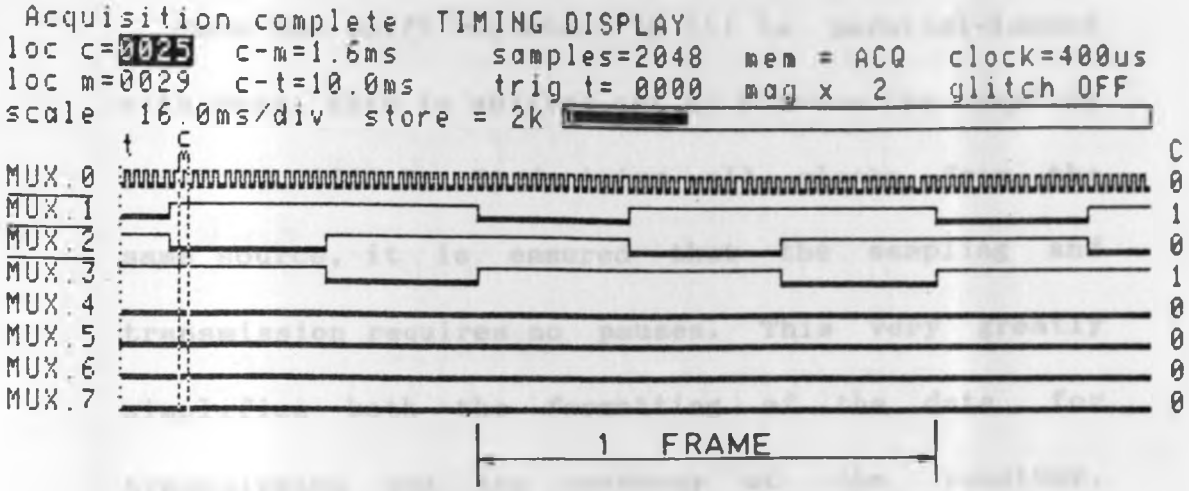


Fig. 6.6 16 x 3 multiplexer control on the C.U. Driver Board. (MUX 0 is the sampling/channel select CK 4).

perfoms A/D conversion by a ramp approximation on IC 3 pin 14. IC 2 is an analogue comparator which compares the input signal with the digital count from IC 3 pin 14. Only when the latter is the higher is the $\overline{\text{DATRDY}}$ line driven LOW by the combination of IC 2 and 4. At the same time, the counting clock for the conversion on IC 3 is disabled. The $\overline{\text{DATRDY}}$ line, while going LOW the instant the A/D conversion is complete, triggers IC 12. This IC is a non-retriggerable monostable which produces a 35ns LOW pulse that parallel-loads shift

register IC 11 with new data. The monostable is used because the $\overline{LD}$ control of IC 11 is level driven.

Once the shift register (IC 11) is parallel-loaded with data, this is shifted out at 8 times the sampling rate *i.e.* 9600 Hz. By deriving all clocks from the same source, it is ensured that the sampling and transmission requires no pauses. This very greatly simplifies both the formatting of the data for transmission and its recovery at the receiver. Otherwise "stuffing" techniques [8] would have to be applied to produce a reliable link. ("Stuffing" involves the insertion of dummy data into the transmission to ensure uniformity of transmission rate). The timing and control information as so far described is shown in Fig. 6.7. Note that a 760 ns minimum time is necessary between the $\overline{DATRDY}$ going LOW and the next positive going 9600 Hz clock edge if the first byte transmitted is to be correct. This time is required to cater for propagation delays and data set-up time in IC's 11 and 12. This sets the minimum limit of the time needed from completion of A/D conversion to beginning of serial transmission.

On Fig. 6.8a and b are shown timing waveforms taken

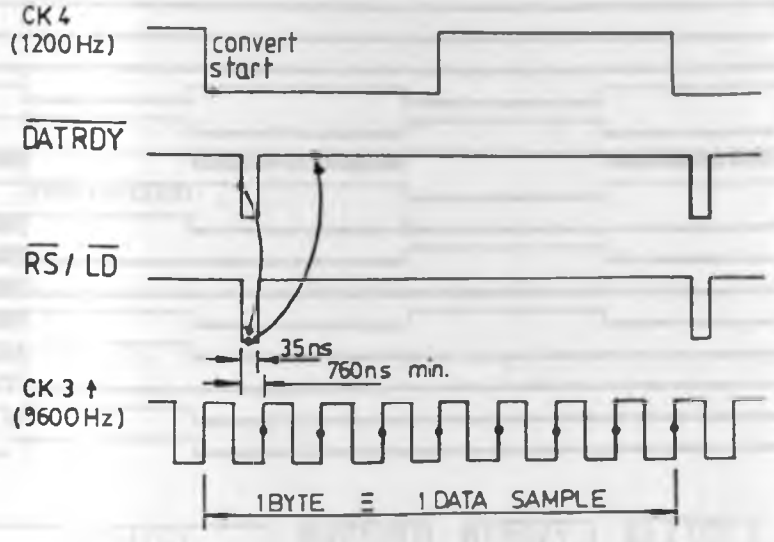


Fig. 6.7 Timing and control on the C.U.

with a Logic Analyser from the C.U.-Data Board in normal operation.

Fig. 6.8a shows the control (CON) and data (DAT) lines. The dark patches represent times when data was changing too fast for the 4μs Logic Analyser clock to resolve. In particular note the 35ns pulse that loads the shift register (CON 0). Also how the input to pin 5 of IC 4b (CON 5) is used to ensure that a conversion takes place only at 1200 Hz and no more often. This ensures that an analogue sample is converted to digital form and read out only in the vicinity of the

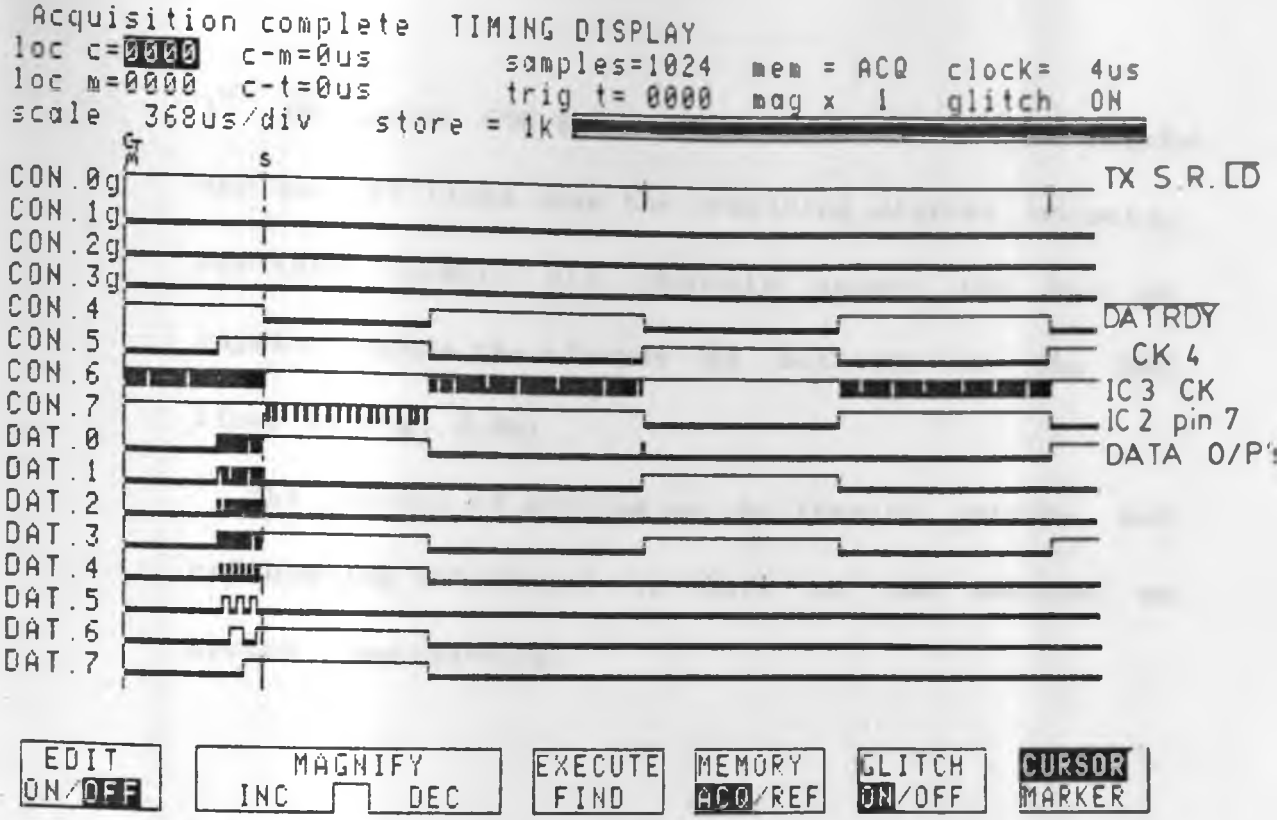


Fig. 6.8a A/D conversion and serial transmission control waveforms, C.U. Data Board.

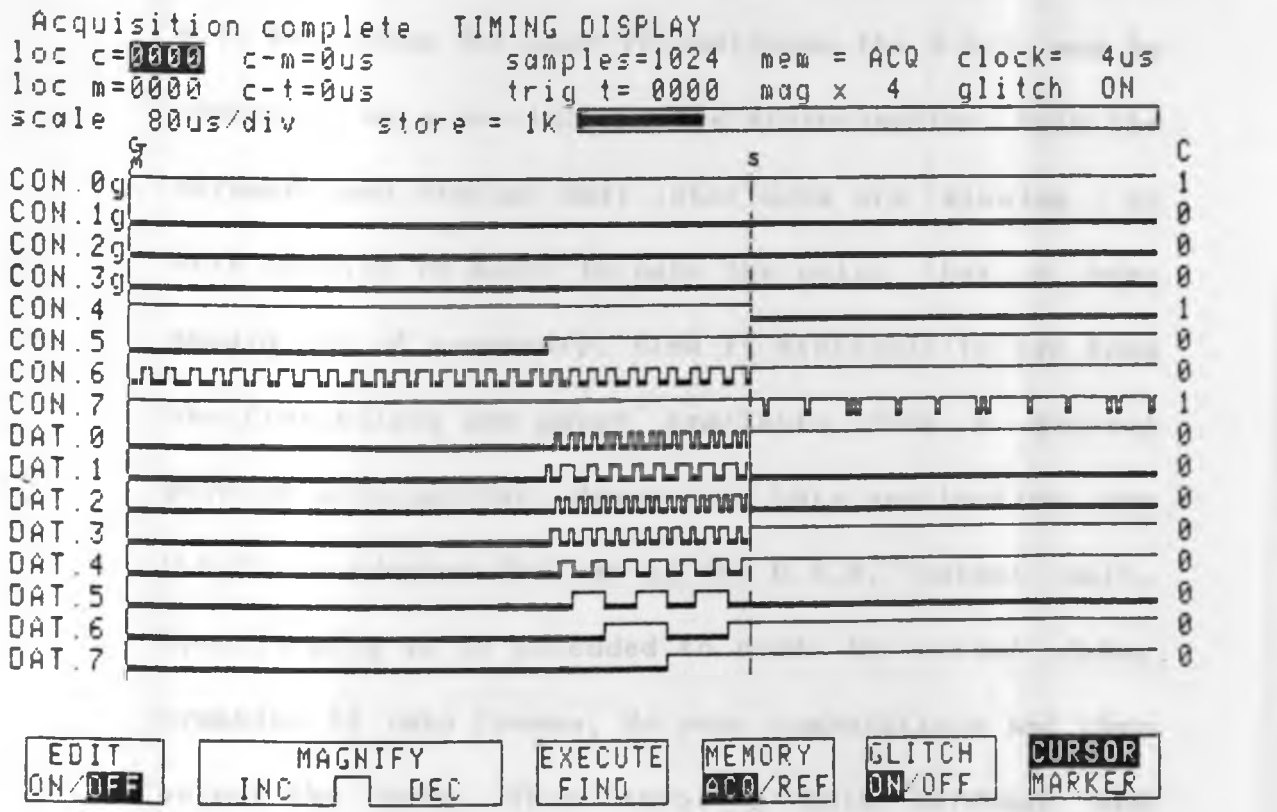


Fig. 6.8b ×4 magnification of Fig. 6.8a showing the start of parallel to serial conversion.

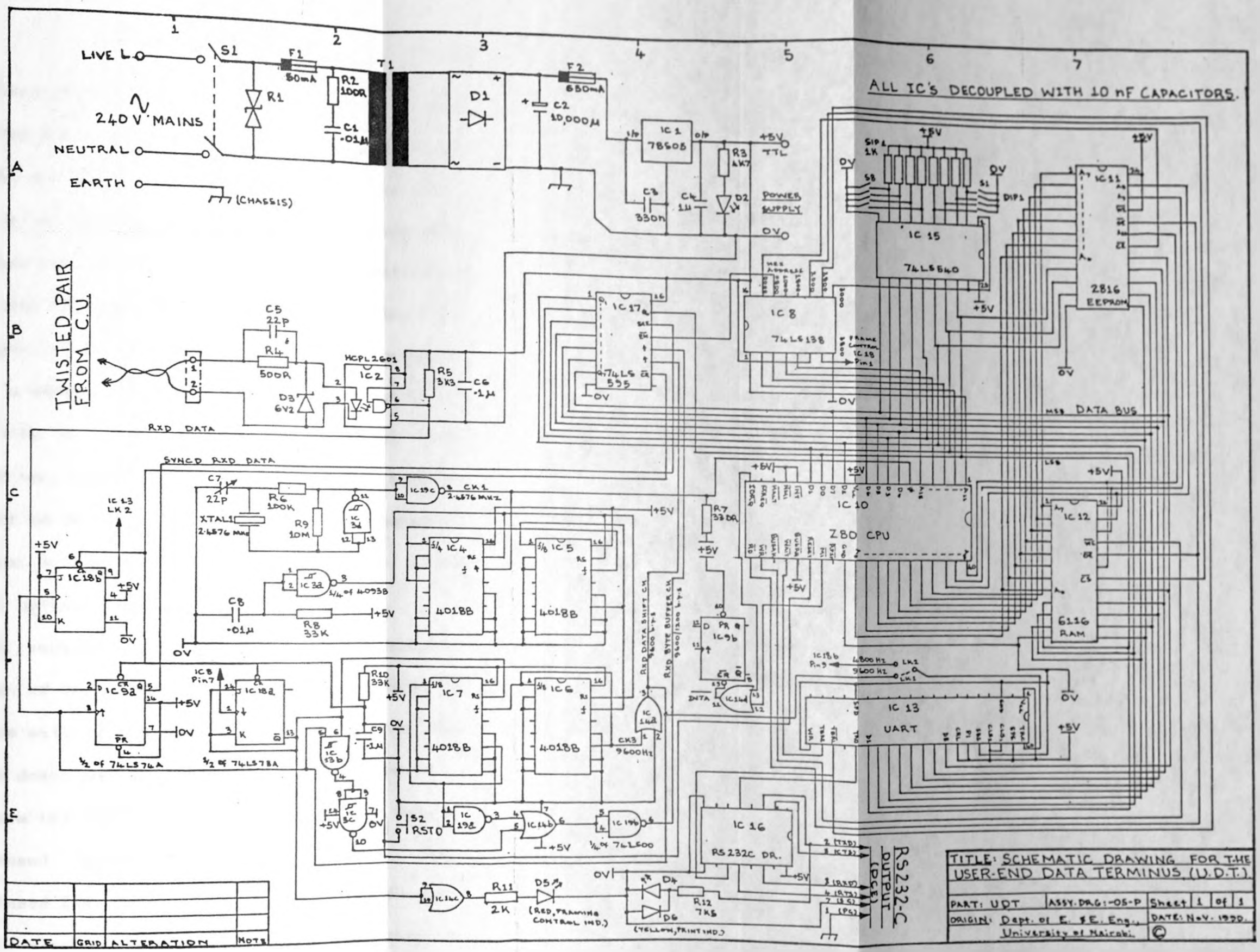


Fig. 6.9 Circuit diagram of the U.D.T.

software functions. In this case the focus is on the hardware. The basis for this is the understanding that the ultimate use of the Unit will be user-specified. Also that unlike hardware the writing of appropriate software does not require a battery of specialised equipment that the user may not have access to. The latter reason led us to concentrate on the hardware because it's design and testing is more constrained from the factories' point of view. This applies also in terms of unavailability of research time, capital and manpower resources and equipment. It is therefore apparent that a clear distinction needs to be drawn between the software and hardware design.

In this section, we describe the hardware functioning of the U.D.T. Although the part played by the software will be mentioned, the specific routines will not be described until the chapter on software.

Apart from the +5V power supply, the U.D.T. has a crystal based clock circuitry and a Z80 processor-based functional block. Clock subdivision produces all clocking required on the board as seen in Fig. 6.9. The processor is supported by 2K-bytes of random access and read only memory each (RAM, ROM). An

8-bit buffered manual switch input is available as are a binary serial receiver register and a universal asynchronous receiver transmitter (UART). It will be clear that the following description of the working of this board nowhere near exhausts its capacity; it merely serves to illustrate a single data acquisition application.

It will be recalled that serial data leaves the C.U.-Data Board at 9600 bits per second (b.p.s.); one byte per analogue channel sample. Also that consecutive bytes come from consecutive channels. The U.D.T. has to perform two essential functions to be a successful receiver. One is to synchronise the arriving bits to its clock so that they are sampled at the right instant. The second is to demarcate the arriving serial train into the appropriate 8-bit words corresponding to each analogue sample. We look at these two problems in turn.

(a) Bit Synchronization.

Data reaching the U.D.T. is received by IC 2, the HCPL 2601 high speed opto-isolator. This affords galvanic isolation of the U.D.T. from the C.U. and protects it in case of high voltages coupling to the

twisted pair carrying the digital signals. Initially, the bit clocks on both the C.U. and U.D.T. are nominally set to the same frequency. Arriving bits are synchronised with the U.D.T. clock by IC 9a (a clocked D-flip-flop) and shifted at 9600 b.p.s. into shift register IC 17. When the receiver is properly framed valid 8-bit data in this shift register is parallel-loaded into the U.D.T. data bus. The system is only correcly framed if this 8-bit data is from the same analogue channel, representing a single sample. Fig. 6.10 shows how the serial data train leaves the transmitter (C.U.) synchronised to its clock. It also shows how the data is synchronised with the positive going edge of the U.D.T. (receiver) bit shifting clock (CK3).

(b) Framing.

The process of properly dividing the serial bit-train into bytes is best depicted in the timing diagrams of Fig. 6.11 as will now be explained. A general picture is given first with more detailed explanations being given in the later paragraphs.

As soon as the U.D.T. is powered and properly initialised, the Processor starts to continuosly read

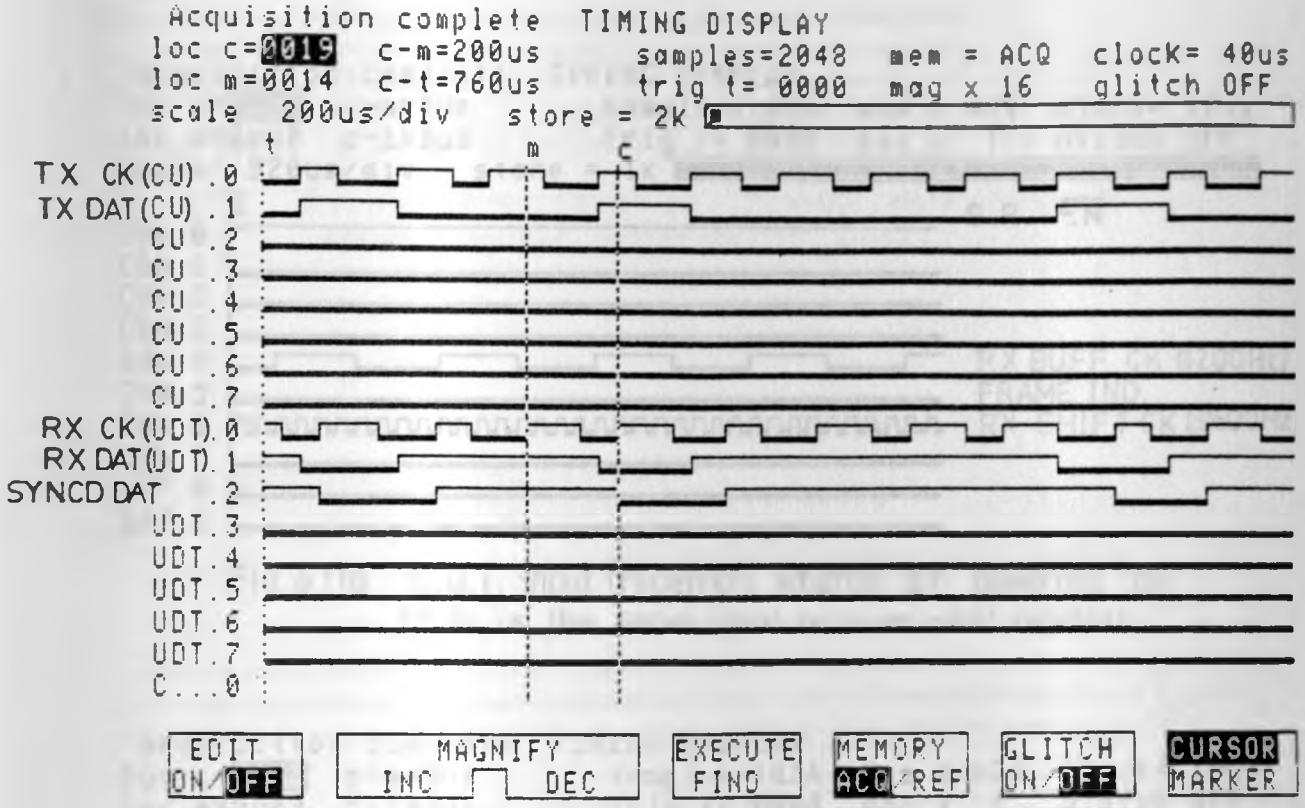


Fig. 6.10 Bit synchronization at the U.D.T.

from the received-data register IC 17. During this time, transmitted serial data is shifted continuously through this register at 9600 b.p.s., equal to the transmit/receive rate. The Processor reads this register until a time when it reads a byte that is identical to an already agreed framing pattern. This tells it that at that instant, and at all other

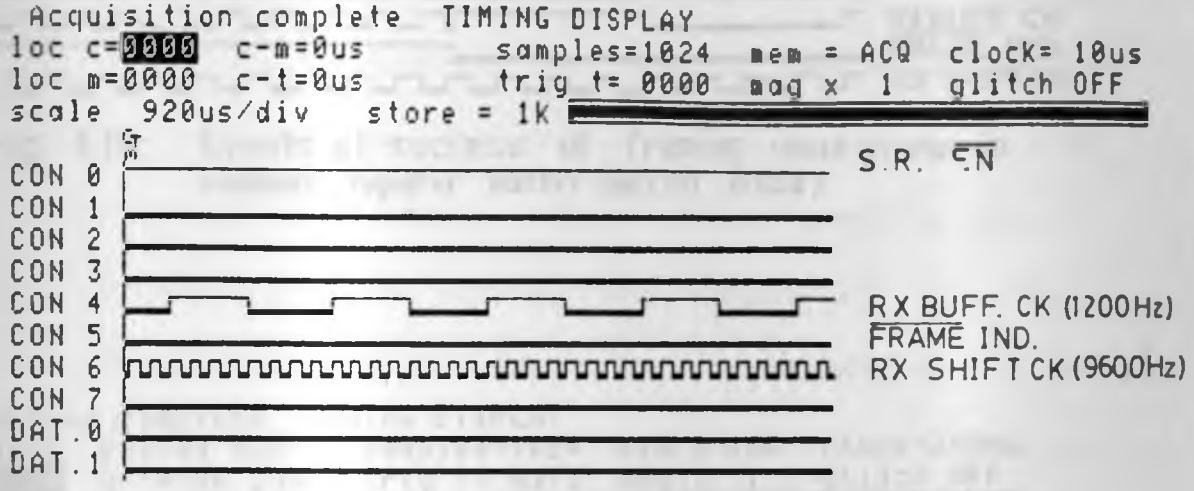


Fig. 6.11a U.D.T. input (receiver) status at powering "on".
(S.R. is the serial input receiver shift register).

Fig. 6.11b Received data framing attempt in progress.

instants separated from it at 1200 Hz, will be available in the receiver register 8-bits of data corresponding to one specific channel only. It also knows that if the framing pattern is taken as channel

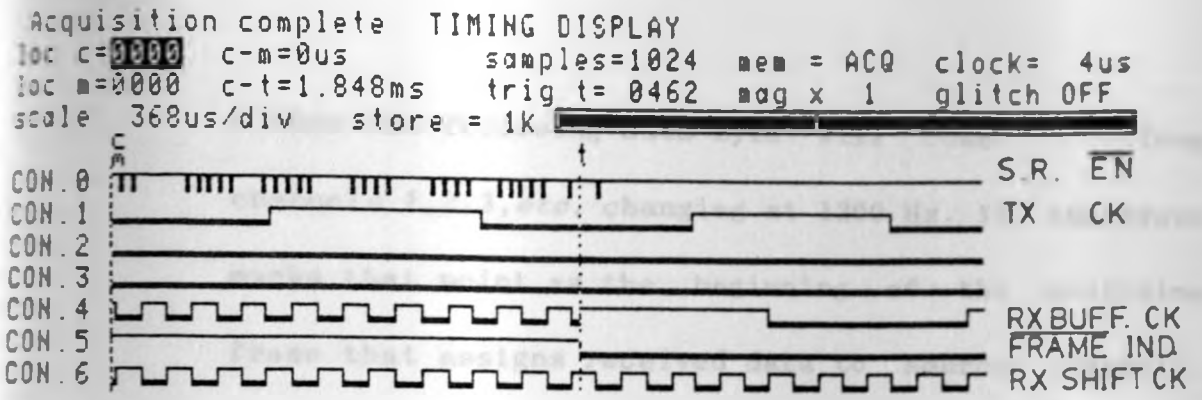


Fig. 6.11c Events at success of framing. (Note change in receiver register buffer control clock).

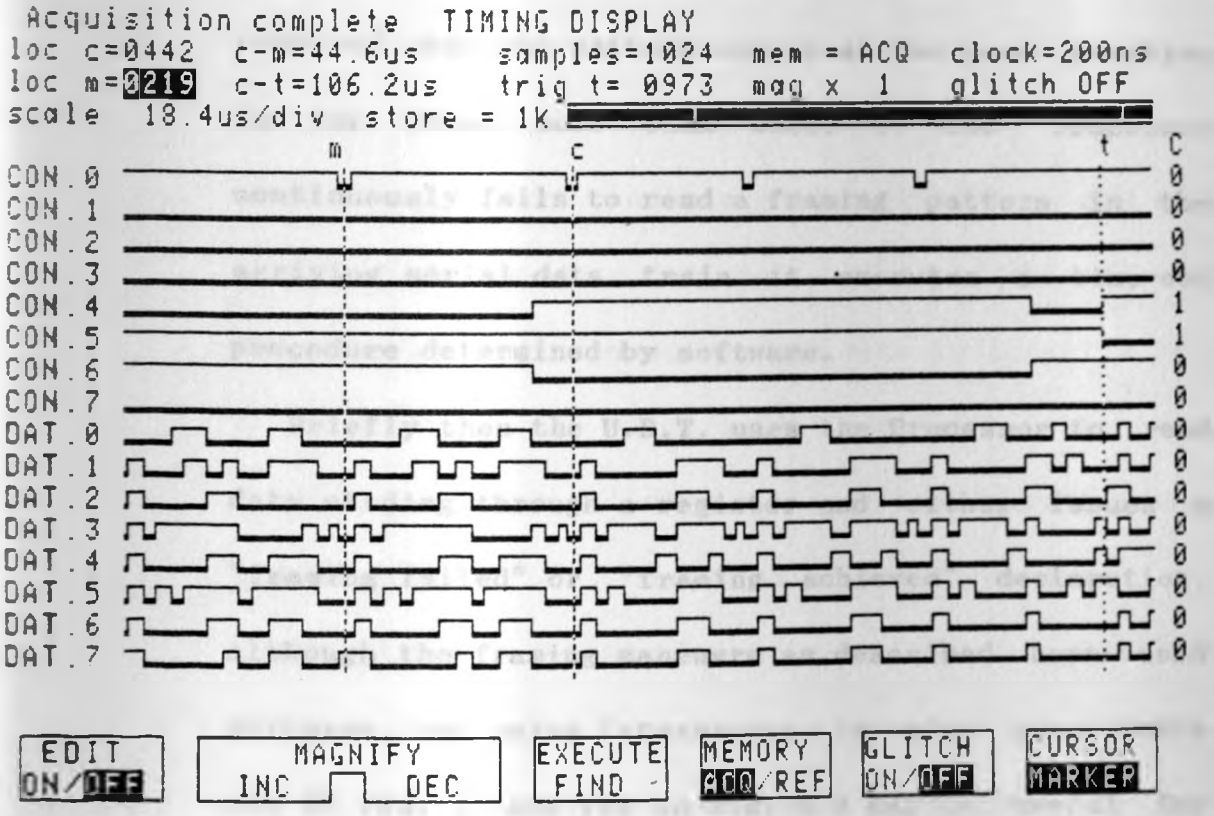


Fig. 6.11d A ×20 magnification of 6.11c. (Note successful capture of the framing pattern 00 H 3 times as required before a framing success is declared). DAT lines show U.D.T data bus contents.

0 then the following data byte will come from channels 1,2,3,*etc.* changing at 1200 Hz. It therefore marks that point as the beginning of the real-time frame that assigns received data to source channels. As explained in the Analysis, the chance of the Processor mistaking a random binary pattern for a framing pattern exists. The probability of this happening is diminished if as a preliminary it is required that the pattern appear at the same position in the frame more than once. If the Processor continuously fails to read a framing pattern in the arriving serial data train it executes a time-out procedure determined by software.

Briefly then the U.D.T. uses the Processor to read data sliding through a register and either issues a "framing failed" or "framing achieved" declaration. Although the framing maneuvre as described here used software, one using interrrupts is also conceivable and IC 18a, 9b and 14d on Fig. 6.9 may be useful for this. They were left in place although a decision not to use interrupts was made to simplify the software.

It is seen that when the Processor declares framing successful, it implies that were data to be read from

the receiver register from then on at 1200 Hz, it would always correspond to the data at the transmitter. In other words, the instant framing is declared, is the right moment to attempt to synchronise the transmitter and receiver framing clocks. These are the 1200 Hz clock that loads the shift register at the transmitter with the 8-bit digital value from an analogue sample; also the clock that unloads the receiver register in the U.D.T. onto the Processor data bus. The objective is to make them appear as if these clocks are identical; from the same source. The Processor declares success of the framing maneuvre by loading a dummy data byte to location 3800 H. This changes the shift/output control on the data receiver register and also extinguishes lamp D5 which indicates when "OFF" that framing has succeeded.

The "framed" declaration effectively separates the shifting and output functions on the receiver register (IC 17). The 74LS595 actually has two clocks, one for shifting data in its register and another for loading data from the register into an output buffer. Before framing, these clocks are tied and data slides continuosly through both. After framing, data is

shifted into the register at 9600 b.p.s. but loaded into the output buffer only at 1200 Hz. In other words the output buffer then holds 8-new bits of valid data every time it is loaded (after framing has been declared successful). This means that at any other time that the processor may read the buffer, data in it will at least correspond to one channel. So in the declaration of framing the processor clocks IC 18a which enables IC 7, disables pin of 5 IC 14 and thereby ensures that the buffer control on IC 17 pin 12 is now driven at 1200 Hz in synchronism with the transmitter sampling clock. More remains to be said about the framing maneuvre but first we explain the waveforms of Fig. 6.11.

Fig. 6.11a shows the situation at the U.D.T. when power has just been supplied but the operator has not initiated the system. CON 1,2 and 3 are not used. CON 0 shows the active low enable line for the received data register IC 17. CON 4 is the byte (buffer) load control for the register. CON 5 is the active low control whose low level indicates framing has been achieved. (It is usually indicating success at switch-on). CON 6 shows the 9600 Hz clock that shifts

a sliding sequence in the receiver register.

Fig. 6.11b shows the situation after U.D.T. initialisation but just before framing is successful. The pulses in CON 0 show the Processor continually reading from the receiver register. CON 5 indicates that framing has not succeeded (HIGH) and CON 4 and 5 are the same clock producing a sliding serial data train into and out of the register and receive buffer in IC 17.

Fig. 6.11c shows the events around the time, t, the framing succeeds. The Processor suddenly stops reading the receiver register (as the software requires), CON 4 the buffer-read clock changes from 9600 Hz to 1200 Hz and CON 5 the framing success indicator goes LOW. CON 1 shows the transmitter framing clock. It should be noted that the shift register clock and the buffer load clock in the receiver register, when tied together before framing succeeds are one clock apart. The latter is always one clock behind. Recall that CON 6 (Fig. 6.11c) is the bit shifting clock in the receiver register while CON 4 is the output buffer clock. It is clear from Fig. 6.11c that after framing is declared at t, the positive going edge of CON 6

shifts eight new bits into the register before CON 4 loads the next 8-bit word into the buffer. (Both CON 4 and CON 6 are positive edge triggering). Although it appears that the eighth bit is shifted by CON 6 simultaneously as the buffer is loaded (which may cause errors on this bit), this is not so. Since the loading (1200 Hz) clock is derived from the shifting (9600 Hz) clock, there is a time delay enforced by the dividing device (counter) between the active edges of these clocks. In this case, the propagation delay introduced by the 4018B counters is at least 200 ns. Since the shift register requires a set up time of 40 ns between these two clocks this requirement is met. Fig. 6.11e clarifies further this shifting sequence.

It is also worthy of note that from the instant the Processor recognises the valid framing pattern in the register, it has at most one period of the bit shifting clock in which to complete the synchronisation procedures. This ensures that it will complete the synchronization before the data it read in the register has been shifted. In this case, this maximum time in which to act is about 100 μs or 256 Processor clock cycles. In practical terms, it means

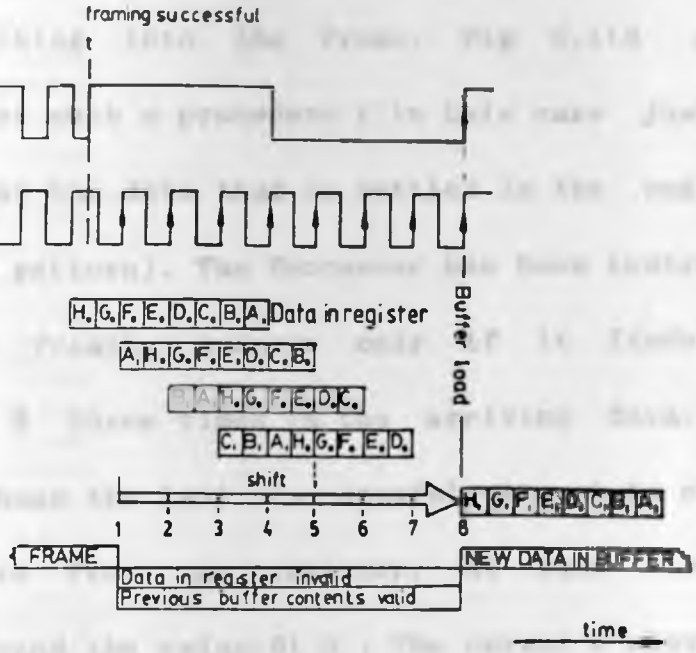


Fig. 6.11e Synchronised byte reconstruction by the U.D.T.

that the software program for the framing maneuvre must be shorter than 256 Processor clocks.

Looking now at Fig. 611d, a x20 magnification of Fig. 6.11c, we see the details of the data on the Processor data bus just before framing is declared at time t. CON 0, CON 4, CON 5 and CON 6 still represent shift register read, buffer read, framing success and data bits shift controls respectively. The DAT waveforms show the data on the bus. As mentioned earlier, the Processsor may be required to find a

certain pattern in the received data several times before locking into the frame. Fig 6.11d shows execution of such a procedure (in this case just to confirm that the data that is settled in the register is a valid pattern). The Processor has been instructed to declare framing success only if it finds the pattern 00 H three times in the arriving data. The marker m shows the last unsuccessful attempt to obtain this pattern from the register. At that time it actually found the value 01 H . The cursor c shows the first successful attempt when it found the value 00 H. The next two attempts were also successful and having found 00 H three times, the Processor executes a framing lock about 36μs later.

Fig 6.12 shows the end result of the transmission process so far described. In particular it shows how digitized data generated from analogue samples in the C.U. is related to data stored in the U.D.T. receiver-register. The "Loc" column refers to the memory location of data in the Logic Analyser. Column "a" shows binary data loaded into the transmitter shift register of the C.U. This is the data that is serially shifted out through the register. Column "a"

```
Acquisition complete   LIST DISPLAY
Loc m=0000 trig t=0007 samples=1024 find=word 1 clock= EXT
       aaaaaaaa bbbbbbbb          c                    (RX SHIFT CK)
Loc      BIN      BIN
0000m 00000000 10100010           0
0001  00000000 01000100           0
0002  00000000 10001000           0
0003  00000000 00010000           0
0004  00001010 00100000           1
0005  00001010 01000000           1
0006  00001010 10000000           1
0007t 00001010 00000000  start    1
0008  00000000 00000000           0
0009  00000000 00000001           0
0010  00000000 00000010           0
0011  00000000 00000101           0
0012  00001001 00001010  valid    1
0013  00001001 00010100           1
0014  00001001 00101000           1
0015  00001001 01010000           1
0016  00000000 10100000           0
0017  00000000 01000001           0
0018  00000000 10000010           0
0019  00000000 00000100           0
0020  00001001 00001001  valid    1
0021  00001001 00010010           1
0022  00001001 00100100           1
0023  00001001 01001000           1
0024  00000000 10010000           0
0025  00000000 00100001           0
0026  00000000 01000010           0
0027  00000000 10000100           0
0028  01010111 00001001  valid    1
0029  01010111 00010010           1
0030  01010111 00100101           1
0031  01010111 01001010           1
0032  00000000 10010101           0
0033  00000000 00101010           0
0034  00000000 01010101           0
0035  00000000 10101011           0
0036  11100001 01010111  valid    1
0037  11100001 10101110           1
0038  11100001 01011101           1
0039  11100001 10111011           1
0040  00000000 01110110           0
a=TXD   b=RXD   c=CLK 4
                (1200 Hz)
```

EDIT ON/OFF | COMPARE ON/OFF | EXECUTE FIND | FIND DIFF | MEMORY ACQ/REF | PAGE UP DOWN

Fig. 6.12 Transmit and Receive register contents after successful setting up of the digital link.

however shows the steady data from the input side of the register where it is not affected by shifting. This data only changes when the A/D converter digitizes a new analogue sample. Bit 0 of column "c" shows the 1200 Hz (sampling)clock. The Logic Analyser acquisitions were driven by the 9600 Hz clock, hence one sees that bit 0 of column "c" is periodic with 8 bits.

Column "b" shows data in the receiver shift register of the U.D.T. Notice particularly that this data is shifted left every 9600 Hz clock. Notice also that when bit 0 column "c" goes from 0 to 1, data in the receiver register (column "b") is identical to the byte in the transmitter register during the previous clock cycle. In other words every positive going edge of the receiver byte-framing clock (1200 Hz) indicates that a valid data byte, corresponding to a digitized analogue sample, is now resident in the receiver register. It is for this reason that the 1200 Hz clock is used to move this byte into the receiver register buffer until such a time as the Processor may wish to read it.

Once valid data is available at the receiver

register it can be said that the function of the acquisition hardware is fulfilled. What the Processor does with this data is an application problem somewhat separate from the issue of its acquisition, transmission and recovery.

In the case of this data acquisition system it was intended that the Processor continuously read and store arriving data and then transfer it for output. To do this, serial RS 232C [26, 27] output transmission in the American Standard Code for Information Interchange (ASCII) format was desired. Thus these two protocals are incorporated in the U.D.T. hardware. U.D.T. software prepares data for output by converting from hexadecimal to ASCII. Output data is loaded into the UART which does the ASCII parallel to serial conversion according to Table 6.1. (This can be rewired according to manufacturer specifications to suit different set-ups). The ASCII data is then fed into the RS 232C line driver IC 16. This IC generates a voltage of at least -5V for HIGH and +5V for LOW to meet this standard. The diode D4 indicates a data output by flashing. Serial data output rate is selectable with LK1,2 either for 300 or

600 bits per second. IC 15 is a buffer for manual inputs from the switches S1-8. It is used in this case to illustrate how the system user can choose the functions to be performed by the D.A.S. software according to the settings of the switches. This is discussed further in the chapter on software. The general function of this addresseable buffer is to avail a window for external devices onto the U.D.T. data bus. But the 74LS540 is unidirectional and would have to be replaced with a bidirectional buffer if two way access is required.

Table 6.1 UART settings.

CONTROL	SETTING	SELECTED
CLS1	HIGH	8-bit characters
CLS2	HIGH	
SBS	LOW	1 stop bit
PI	HIGH	No parity

It aught to be mentioned that the addressing structure of the U.D.T. is not completely decoded. It will, in fact be seen that a somewhat liberal approach was taken in the use of memory space. For example, the locations 3800 H to 3FFF H are taken up by the framing

control line. The main reason for this is that memory size in this case had to be compromised with the cost of decoding. This includes not only the cost of the decoding IC's but also the printed circuit board (pcb) real estate. It was considered that the D.A.S. was not intended to be a data processing system but rather one that reads in and outputs data in real time. Thus RAM size was not considered a variable to be maximized at whatever cost. ROM size is determined directly by the length and variety of the system routines required to be resident in the D.A.S. Their length is determined by their data processing sophistication while the number of routines is related to the variety of different tasks the D.A.S. may be required to perform. It was considered that the critical minimum size of ROM must be able to store a useful D.A.S. software operating system and at least a few application routines. These are the minimum required to enable the D.A.S. to be used either as a stand alone unit or as a satellite of a PC-based data processing system. With these in mind, 2 Kbytes of RAM and EEPROM each was installed. A further 4K of memory expansion can be added very easily and is therefore available in

reserve.

In summary, the U.D.T. may be considered as an "intelligent" receiver of serial data with operator programmability and a computer compatible RS 232C bus output. According to the definition of the Comité Consultatif International Télégraphique et Téléphonique (CCITT), [27] the U.D.T. is connected as a data circuit-terminating equipment (DCE) in half-duplex mode.

In Section 6.4 we very briefly review the major points covered in this chapter about the hardware realization of the D.A.S.

6.4 Hardware Review.

Realization of possible functional units of the D.A.S. analysed in Parts I and II has been described. It has been emphasized that this implementation is considered optimum only for this case study. The analytical process of Parts I and II may be used to arrive at the optimal hardware solution to other specific situations. Nevertheless it is expected that the illustration presented in Chapter 6 is general enough for adaptation to most situations with minimal

effort. Fig. 6.13 shows the main D.A.S. functional blocks.

It has been shown how the performance of the hardware in the D.A.S. was tested to ascertain its meeting of design targets. The objective here has been to show that the prototype hardware behaves as expected; in particular that analogue processes meet theoretical predictions and that digital data transmission can be effected with integrity. Having established these we will shortly discuss the practical issues of system integration, calibration and output interfacing in Chapter 8. But before that we address the software aspects in Chapter 7.

Note on Power Supplies:

Power supply voltage output from all D.A.S. units takes on the typical RC first order decay after mains power "OFF". On full load the following time constants apply for output voltage decay from the nominal value: 95% , 100 ms and 50% 400 ms.

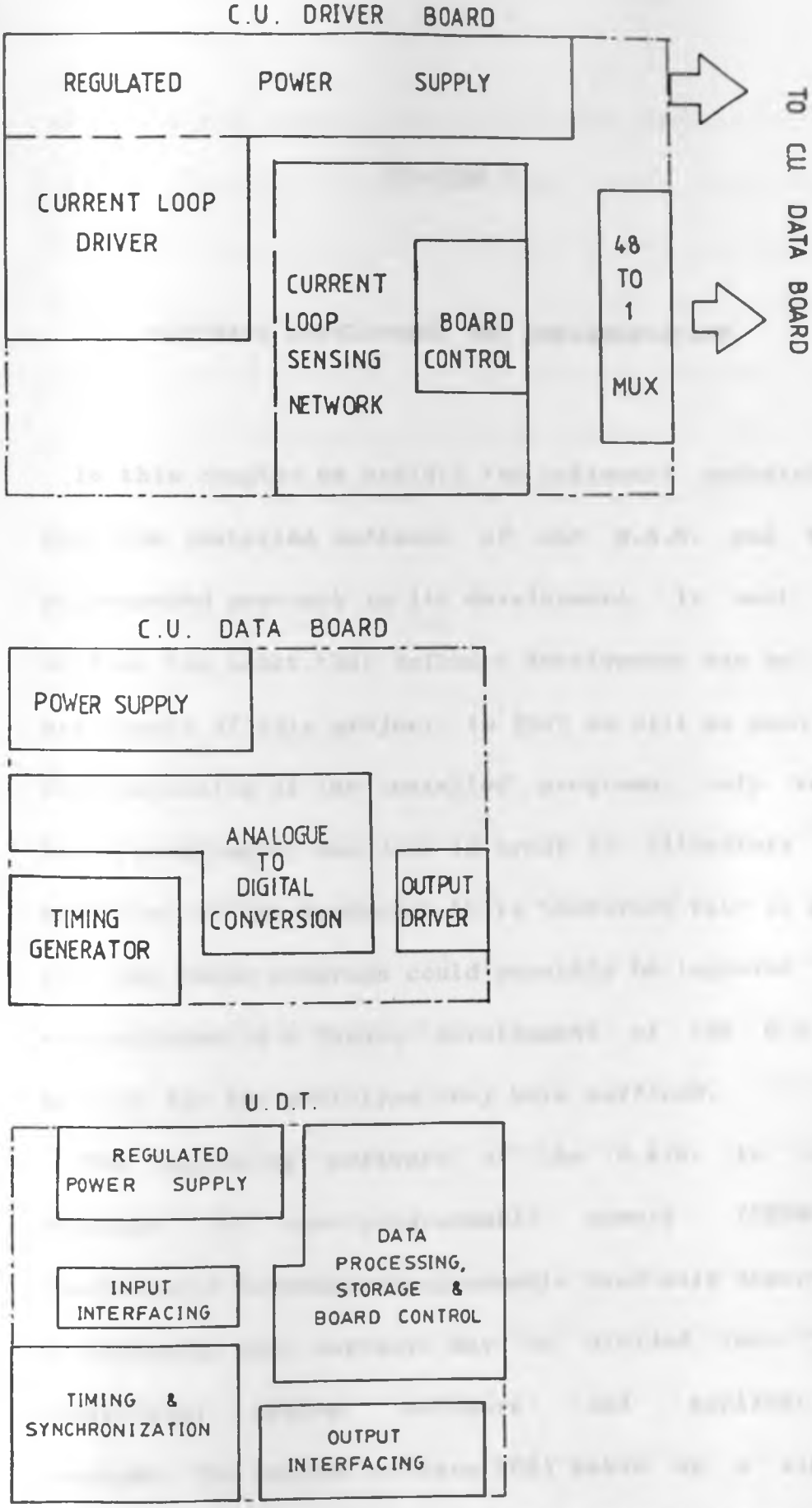


Fig. 6.13 Functional blocks of main D.A.S. circuits.

CHAPTER 7

SOFTWARE DEVELOPMENT AND IMPLEMENTATION

In this chapter we explain the rationale underlying both the installed software of the D.A.S. and the recommended approach in its development. It must be said at the onset that software development was not a key aspect of this project. In fact as will be seen in the discussion of the installed programs, only very basic programming was done in order to illustrate the behaviour of the hardware. It is therefore fair to say that all these programs could possibly be improved or restructured in a future development of the D.A.S. However for the prototype they have sufficed.

The operating software of the D.A.S. is all resident in user-programmable memory (EEPROM: electrically eraseable-programmable read only memory). Conceptually this software may be divided into two categories; system software and application programs. The system software (OS) makes up a simple Operating System for the U.D.T. It initializes the

system by for example clearing the RAM, reading in the operator settings and executing the acquisition maneuvre. The application programs are essentially data processing routines. For example the routine "SAMPIN" reads in data from the receiver register and stores it in an operator selected region of RAM. We discuss these two software functions separately.

7.1 Software Description.

(a) System Software.

The objectives defined for system software were that it be able to support the demonstration of the working of the hardware and the desired application programs. A further objective was that it enables a user to continuously install new routines without having to interfere with previous ones. Fig. 7.1 shows the basic configuration of the U.D.T. software structure. The higher the program on the page, the earlier it comes in execution which means that lower programs must be called by higher ones. Programs on the same horizontal line are subroutines of the preceeding program.

The operating system starts with COLD.SYS and ends

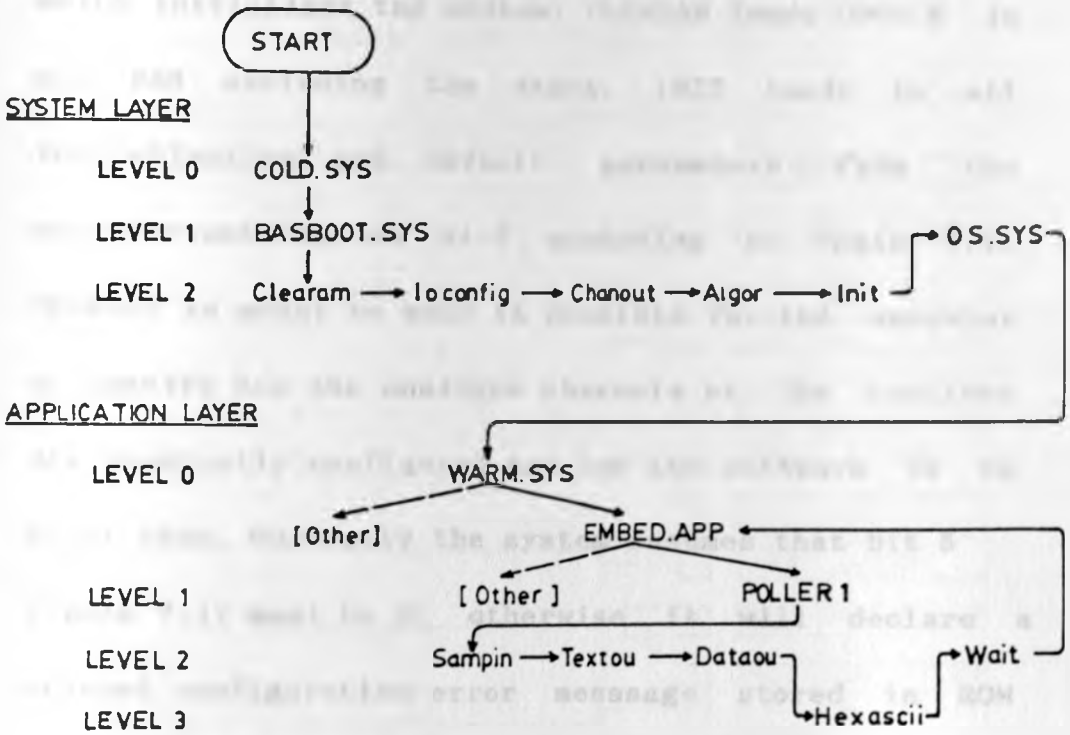


Fig. 7.1 D.A.S. software structure.

when an operator pre-selected routine is chosen for the application software in the selector routine OS.SYS. A listing of the whole software in EEPROM is shown at the end of this chapter. Following is a description of the operating system functions in COLD.SYS.

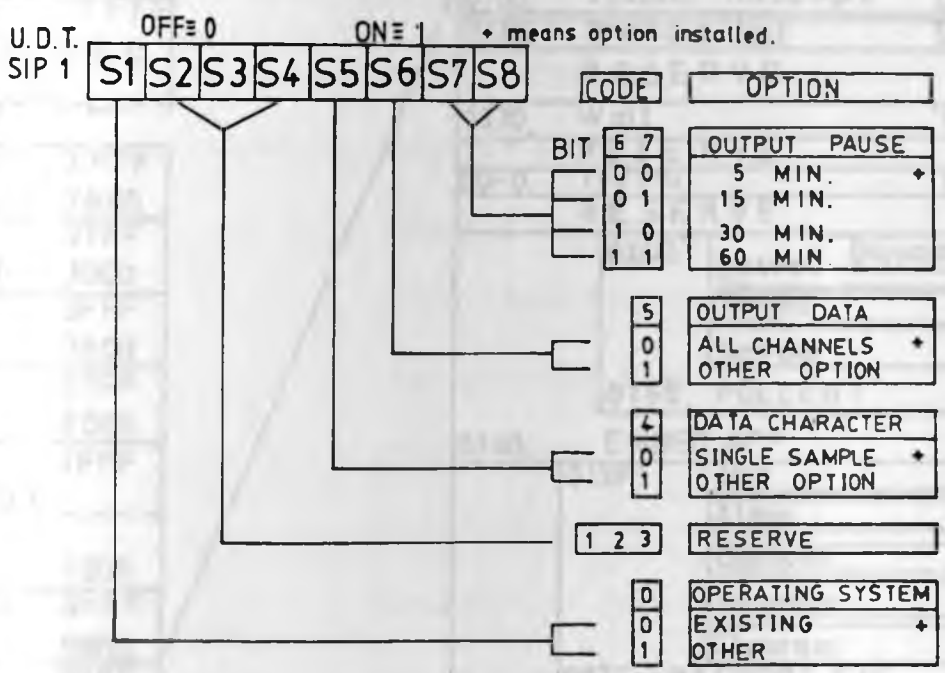
COLD.SYS starts by disabling maskable

interrupts and then moves to set up a stack from location 207D H (The area 2000 H-207D H is reserved for the stack). The program then calls BASBOOT.SYS which initialises the system: CLEARAM loads 0000 H in all RAM excluding the stack. INIT loads in all initialization and default parameters from the operator settings on S1-8 according to Table 7.1. CHANOUT is meant to make it possible for the operator to specify how the analogue channels at the receiver are physically configured and how the software is to treat them. Currently the system assumes that bit 5 (Table 7.1) must be 0, otherwise it will declare a channel configuration error messsage stored in ROM addresses 0640 H to 061C H. Similarly ALGOR is used to point to the chosen data processing (application) routine and is currently expected to have bit 4 (Table 7.1) set to 0. Its error message is the same as that of CHANOUT. IOCONFIG is used to specify the real-time output properties of the system from the operator settings according to Table 7.1. However only the 5 minute periodic output is installed and bits 6 and 7 are therefore defaulted as both zero.

After execution of these routines, the system cold

start is considered over and control is handed over to

Table 7.1 Manual switch settings on U.D.T.



the routine OS.SYS which finds out from the operator settings what the required application software package is. OS.SYS then hands over control to the selected main program (package) which itself is essentially a directory.

The COLD.SYS routines, particularly INIT store global variables in RAM that are later used by

application programmes. Fig.7.2 and Table 7.2 show the

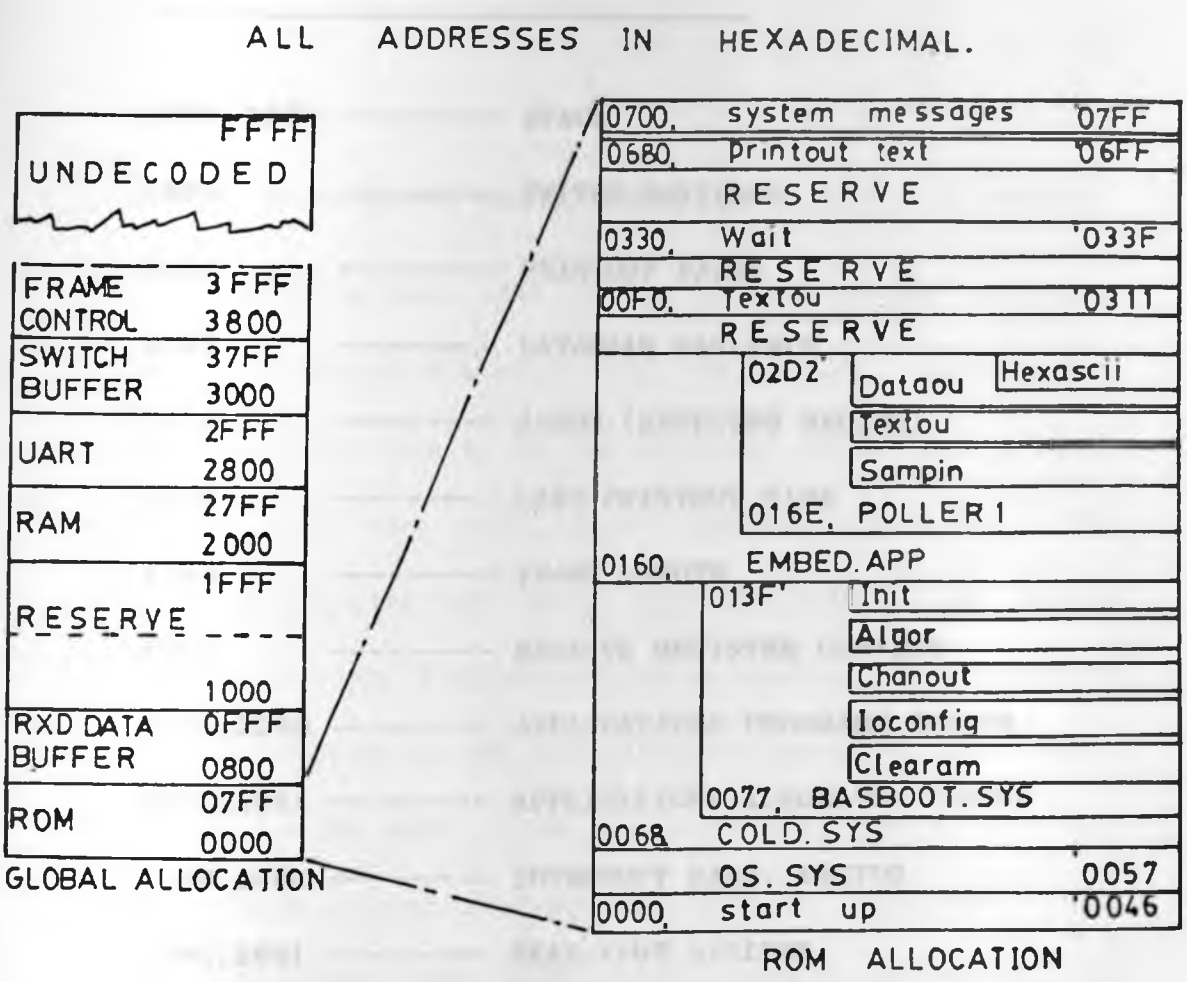


Fig. 7.2 D.A.S. memory map.

system memory map and reserved locations in ROM and RAM. Although an attempt is made to make single programs fit contiguously, this is not entirely possible and consecutive lines in the program may

Table 7.2 Reserved RAM locations.

Location (HEX)	Value Stored
2000-207F	STACK
2080	SWITCH SETTINGS
2081	PRINTOUT PAUSE
2082	DATACHAR VARIABLE
2083	ALGOR (SAMPLING REGIME)
2084	LAST PRINTOUT TIME
2085	FRAME LENGTH
2086	RECEIVE REGISTER CONTENT
2087,2088	APPLICATIONS PROGRAMS VECTOR
2089,208A	APPLICATIONS ALGORITHM VECTOR
208B,208C	INTERRUPT HAND. VECTOR
2090,2091	REAL-TIME DIVIDER
2092	SECONDS COUNT
2093	MINUTES COUNT
2094	HOURS COUNT
2095	ANALOG CHANNELS SYMBOL
2096	PULSE CHANNELS SYMBOL
20FE	IDENTITY OF CURRENT CHANNEL
27FE	LAST CHANNEL READ

27FF --------- FRAMING LOCK CONSTANT

27F0- --------- 1st SAMPLE CAPTURED DATA

27C1 --------- 48th SAMPLE CAPTURED DATA

actually reside at quite separate locations in memory.

It will be seen that in RAM the installed software has only reserved space for the stack, application constants written in by the program INIT for global system use and application indices used by the application programs based around SAMPIN. By using Table 7.1 in conjuction with INIT, an extensive re-structuring of the installed software is possible. In ROM on the other hand, space is reserved at the top for system (error) message manipulator routines *i.e.* the routines that deal with errors detected in executing software. In this case if a fatal error (like the operator selecting a non-existent data processing routine) is detected, the system will simply print out a message stored in the "System Messages" part of ROM . The main application program WARM.SYS can be configured to support a vectoring response to Z80 interrupt M1 which sends the Processor

program counter to location 0038 H. The U.D.T. response to interrupt M1 can be placed at any location indicated by the address stored (by INIT) at locations 208B H (low byte) and 208C H (high byte). The application routines now to be described are however not interrupt-based.

(b) Application Software.

With the cold start over, OS.SYS hands over control to the main application program WARM.SYS which itself may hand over to another program. In this case it is assumed that interrupt based and polling based data read-in routines are completely separate, and the choice of one or the other is taken in WARM.SYS. The next level of installed application software EMBED.APP calls specialised function routines at even lower level. In this case, EMBED.APP calls POLLER1 which serves as the first routine in the actual data manipulating programs. POLLER1 performs the role of acquiring the framing pattern and synchronizing the received data to the transmitter. It then declares a "framing locked" and may then call a time generating

routine. In this case POLLER1 calls SAMPIN which reads one frame of data from the receiver register into RAM. This done, POLLER1 calls TEXTOU, a program that reads header text from ROM to precede a data print-out. Then the program DATOU is asked to read the data stored in RAM and send it out to the UART after converting it from hexadecimal to ASCII. (To do this conversion, DATOU calls its own subroutine HEXASCII).

The UART reads the parallel data offered to it,converts it into serial bits, adds start, parity and stop bits and loads it onto the RS 232C line driver. When this process is over, POLLER1 calls another routine to find out what to do next. In this case the routine is WAIT which just executes a waiting sequence that lasts about 5 minutes. Then it requests the Processor to read in new data and re-execute the sequence of events. Thus effectively a dedicated hard-copy printing device is updated with process data through the RS 232C bus every 5 minutes.

It is hoped that the foregoing suffices in explaining the basic structure of the embedded programs. It will perhaps be noted that the processing power of the Z80 is hardly exhausted. Also that the

aim has not been to delve into the development of optimal real-time software. This is critically task-specific in all situations where extensive processing is desired and is not included in this brief. Some of the texts listed in the Bibliography refer to this subject . It will also be seen that program elegance has occasionally been sacrificed for the sake of functional clarity, say in the use of labelled jump instructions. However it is hoped that the programs illustrate succinctly how D.A.S. hardware and software interact.

In Section 7.2 is listed the software (firmware) installed and operating as described. NOP instructions appearing in the programs were generally used to obviate the need to change program listing (after changes) rather than for timing purposes. The need to limit program changes arose out of severe difficulties with software development. This is discussed in Chapter 8.

7.2 D.A.S SOFTWARE LISTING.

a. System Firmware .

L E V E L 0

PROGRAM/Comment	PC HEX	ASSEMBLER	STATES	ROM ADD	OPCODE
COLD.SYS	0001	RST 0	11	0000	C7
	0002	DI	4	0001	F3
	0004	IM1	11	0002	ED 56
	0040	JP 0040	10	0004	C3 40 00
	0043	RST 0	11	0038	C7
Set up Stack	0043	LD SP 207D	13	0040	31 7D 20
Go to BASBOOT.SYS	0068	JP 0068	8	0043	C3 68 00
OS.SYS	0049	LD A (2080)	13	0046	3A 80 20
	004B	BIT 0 A	8	0049	CB 47
To error handler	004E	JP NZ 07C0	10	004B	C2 C0 07
	0051	LD A (2087)	13	004E	3A 87 20
	0052	LD L A	4	0051	6F
	0055	LD A (2088)	13	0052	3A 88 20
	0056	LD H A	4	0055	67
Warm operat.vect.	0057	PUSH HL	11	0056	E5
To WARM.SYS	0160	RET	10	0057	C9

L E V E L 1

BASBOOT.SYS	0080	CALL 0080	17	0068	CD 80 00
	0092	CALL 0092	17	006B	CD 92 00
	00C0	CALL 00C0	17	006E	CD C0 00
	00D8	CALL 00D8	17	0071	CD D8 00
	00F0	CALL 00F0	17	0074	CD F0 00
Return to OS.SYS	0046	JP 0046	10	0077	C3 46 00

L E V E L 2

CLEARAM	0083	LD HL 2080	10	0080	21 80 20
	0085	LD C 0080	7	0083	0E 80
	0087	LD D 0F	10	0085	16 0F
	0088	NOP	4	0087	00
	008A	LD (HL) 00	10	0088	36 00
	008B	INC HL	4	008A	23
	008C	DEC D	6	008B	15
	008E	JR NZ FA	8/13	008C	20 FA
	008F	DEC C	4	008E	OD
	0091	JR NZ F4	7/12	008F	20 F4
	006B	RET	10	0091	C9

IOCONFIG	0095	LD A (3000)	13	0092	3A 00 30
	0098	LD (2080) A	13	0095	32 80 20
	009A	BIT 6 A	8	0098	CB 77
	009C	JR NZ 10	7/12	009A	20 10
	009E	BIT 7 A	8	009C	CB 7F
	00A0	JR NZ 06	7/12	009E	20 06
	00A2	LD A 05	7	00A0	'3E 05
	00A5	LD (2081) A	13	00A2	32 81 20
	006E	RET	10	00A5	C9
	00A8	LD A 0F	7	00A6	3E 0F
	00AB	LD (2081) A	13	00A8	32 81 20
	006E	RET	10	00AB	C9
	00AE	BIT 7 A	8	00AC	CB 7F
	00B0	JR NZ 06	7/12	00AE	20 06
	00B2	LD A 1E	7	00B0	3E 1E
	00B5	LD (2081) A	13	00B2	32 81 20
	006E	RET	10	00B5	C9
	00B8	LD A 3C	7	00B6	3E 3C
	00BB	LD (2081) A	13	00B8	32 81 20
	006E	RET	10	00BB	C9
CHANOUT	00C3	LD A (3000)	13	00C0	3A 00 30
	00C6	LD (2080) A	13	00C3	32 80 20
	00C8	BIT 5 A	8	00C6	CB 6F
To error handler	00CB	JP NZ 0740	10	00C8	C2 40 07
	00CD	LD A 00	7	00CB	3E 00
	00D0	LD (2082) A	13	00CD	32 83 20
	0071	RET	10	00D0	C9
ALGOR	00DB	LD A (3000)	13	00D8	3A 00 30
	00DE	LD (2080) A	13	00DB	32 80 20
	00E0	BIT 4 A	8	00DE	CB 67
To error handler	00E3	JP NZ 0740	10	00E0	C2 40 07
	00E5	LD A 00	7	00E3	3E 00
	00E8	LD (2083) A	13	00E5	32 83 20
	0074	RET	10	00E8	C9
INIT	00F0	LD A 60	10	00F0	3E 60
	00F5	LD (2087) A	13	00F2	32 87 20
	00F7	LD A 01	10	00F5	3E 01
	00FA	LD (2088) A	13	00F7	32 88 20
	00FC	LD A 6E	10	00FA	3E 6E
	00FF	LD (2089) A	13	00FC	32 89 20
	0101	LD A 01	10	00FF	3E 01
	0104	LD (208A) A	13	0101	32 8A 20
	0106	LD A 01	10	0104	3E 01
	0109	LD (27FF) A	13	0106	32 FF 27
	010B	LD A 41	10	0109	3E 41
	010E	LD (2095) A	13	010B	32 95 20
	0110	LD A 44	10	010E	3E 44
	0113	LD (2096) A	13	0110	32 96 20
	0115	LD A 30	10	0113	3E 30
	0118	LD (2085) A	13	0115	32 85 20
	011A	LD A 19	10	0118	3E 19
	011D	LD (2090) A	13	011A	32 90 20

```
                011F   LD A 00              10      011D   3E 00
                0122   LD (2091) A          13      011F   32 91 20
                0126   LD IX 27F0           14      0122   DD 21 F0
                0128   LD A C0              10      0126   3E C0
                012B   LD (207D) A          13      0128   32 7D 20
                012D   LD A 07              10      012B   3E 07
                0130   LD (207E) A          13      012D   32 7E 20
                0131   NOP                   4      0130   00
                0132   NOP                   4      0131   00
                0135   JP 0135              10      0132   C3 35 01
                0137   LD A 30              10      0135   3E 30
                013A   LD (27FE) A          13      0137   32 FE 27
                0077   RET                  10      013A   C9

                       ERROR HANDLING ROUTINES

OSFAIL          07C4   LD IX 0680           14      07C0   DD 21 80
                07C7   LD A (IX+0)          19      07C4   DD 7E 00
                07C9   CP 00                 7      07C7   FE 00
                07CB   JR Z 07             7/12      07C9   28 07
                07CE   LD (2800) A          13      07CB   32 00 28
                07D0   DEC IX               10      07CE   DD 2B
                07D2   JR F2                12      07D0   18 F2
Re-attempt start 0160  JP 0160              10      07D0   C3 60 01

ALGFAIL         0744   LD IX 0640           14      0740   DD 21 40
Error message out 07C4 JP 07C4              10      0744   C3 C4 07

FRAMFAIL        0784   LD IX 0660           14      0780   DD 21 60
Error message out 07C4 JP 07C4              10      0784   C3 C4 07

                                      E   N   D
```

b. Application Firmware

```
                L   E   V   E   L       0

WARM.SYS        0163   LD A (2089)          13      0160   3A 89 2(
                0164   LD L A                4      0163   6F
                0167   LD A (208A)          13      0164   3A 8A 2(
                0168   LD H A                4      0167   67
                0169   PUSH HL              11      0168   E5
                016E   RET                  10      0169   C9

                L   E   V   E   L       1

POLLER1         0171   LD HL FFFF           10      016E   21 FF F
                0174   LD A (27FF)          13      0171   3A FF 2
                0175   LD B A                4      0174   47
                0178   LD A (0800)          13      0175   3A 00 0
                017A   CP F5                 7      0178   FE F5
```

	017C	JR Z 09	7/12	017A	28 09
	017D	DEC HL	6	017C	2B
	017E	LD A H	4	017D	7C
	0180	CP 00	7	017E	FE 00
	0182	JR NZ F3	7/12	0180	20 F3
Framing failed	0185	JP 0780	10	0182	C3 80 07
	0187	DJNZ EE	8/13	0185	10 EE
	018A	LD (3800) HL	13	0187	22 00 38
Call SAMPIN	0200	CALL 0200	17	018A	CD 00 02
Call TEXTOU	02F0	CALL 02F0	17	018D	CD F0 02
Call DATOU	0257	CALL 0257	17	0190	CD 57 02
Call WAIT	0330	CALL 0330	17	0193	CD 30 03
Return to WARM.SYS	0160	JP 0160	10	0196	C3 60 01

L E V E L 2

SAMPIN	0204	LD IX 27F0	14	0200	DD 21 F0
	0207	LD A (27FE)	13	0204	3A FE 27
	0208	LD B A	4	0207	47
	020B	LD A (2083)	13	0208	3A 83 20
	020D	CP 00	7	020B	FE 00
To error handler	0210	JP NZ 0740	7/12	020D	C2 40 07
	0213	LD A (0800)	13	0210	3A 00 08
	0216	LD (IX+0) A	19	0213	DD 77 00
	0219	LD A (2095)	13	0216	3A 956 2
	021A	LD C A	7	0219	4F
	021D	LD A (2096)	13	021A	3A 96 20
	0220	LD (2095) A	13	021D	32 95 20
	0221	LD A C	7	0220	79
	0224	LD (2096) A	13	0221	32 96 20
	0226	DEC IX	23	0224	DD 2B
	0228	DJNZ 01	8/13	0226	10 01
Back to POLLER1	018D	RET	10	0228	C9
	022A	LD A B	4	0229	78
	022D	LD (27FE) A	13	022A	32 FE 27
	022F	LD B 0F	7	022D	06 0F
	0230	LD C 07	7	022F	0E 07
	0231	DEC C	6	0231	0D
	0233	JR NZ FD	7/12	0232	20FD
(See Note:1)	0235	DJNZ FA	8/13	0234	10 FA
Next sample	0210	JR D9	12	0236	18 C3
TEXTOU	02F3	LD A (2093)	13	02F0	3A 93 2
	02F7	LD IX 2081	14	02F3	DD 21 8
	02FA	LD HL 2084	10	02F7	21 84 2
	02FC	CP 00	7	02FA	FE 00
	02FE	JR 06	7/12	02FC	18 06
	02FF	SUB (HL)	7	02FE	96
	0302	CP (IX+0)	19	02FF	DD BE 0
	0305	JP 0305	10	0302	C3 05 0
	0308	LD HL 0700	10	0305	21 00 0
	030A	LD B 80	7	0308	06 80

	030B	LD A (HL)	7	030A	7E
	030E	LD (2800) A	13	030B	32 00 28
	030F	DEC HL	6	030E	2B
	0311	DJNZ F9	8/13	030F	10 F9
Back to POLLER1	0190	RET	10	0311	C9
DATOU	0259	LD D 30	7	0257	16 30
	025D	LD IX 0260	14	0259	DD 21 60
	0260	LD HL 27F0	10	025D	21 F0 27
	0261	NOP	4	0260	00
	0264	LD A (2085)	13	0261	3A 85 20
	0265	SUB D	4	0264	92
	0267	ADD A 30	7	0265	C6 30
	026A	LD (2800) A	13	0267	32 00 28
	026C	LD B 07	7	026A	06 07
	026E	LD A 20	7	026C	3E 20
	0271	LD (2800) A	13	026E	32 00 28
	0273	DJNZ F9	8/13	0271	10 F9
	0276	LD A (2095)	13	0273	3A 95 20
	0279	LD (2800) A	13	0276	32 00 28
	027A	LD C A	4	0279	4F
	027D	LD A (2096)	13	027A	3A 96 20
	0280	LD (2095) A	13	027D	32 95 20
	0281	LD A C	4	0280	79
	0284	LD (2096) A	13	0281	32 96 2
	0286	LD B 07	7	0284	06 07
	0288	LD A 20	7	0286	3E 20
	028B	LD (2800) A	13	0288	32 00 2
	028D	DJNZ F9	8/13	028B	10 F9
Call HEXASCII	029A	CALL 029A	17	028D	CD 9A 0
Return to POLLER1	0193	RET	10	0290	C9
WAIT	0332	LD C B0	7	0330	0E B0
	0334	LD D F7	7	0332	16 F7
	0336	LD E C7	7	0334	1E C7
	0337	DEC E	6	0336	1D
	0339	JR NZ FD	7/12	0337	20 FD
	033A	DEC D	6	0339	15
	033C	JR NZ F8	7/12	033A	20 F8
	033D	DEC C	6	033C	0D
(See Note:2)	033F	JR NZ F3	7/12	033D	20 F3
Acquire new data	0196	RET	4	033F	C9

L E V E L 3

HEXASCII	029B	LD A (HL)	7	029A	7E
	029D	LD B 04	7	029B	06 04
	029F	SRL A	8	029D	CB 3F
	02A1	DJNZ FC	8/13	029F	10 FC
	02A3	ADD A 30	7	02A1	C6 30
	02A5	CP 3A	7	02A3	FE 3A
	02A8	JP M 02AA	10	02A5	FA AA
	02AA	ADD A 07	7	02A8	C6 07
	02AD	LD (2800) A	13	02AA	32 00
	02AE	LD A (HL)	7	02AD	7E
	02B0	AND 0F	7	02AE	E6 0F

	02B2	ADD A 30	7	02B0	C6 30
	02B4	CP 3A	7	02B2	FE 3A
	02B7	JP M 02B9	10	02B4	FA B9 02
	02B9	ADD A 07	7	02B7	C6 07
	02BC	LD (2800) A	13	02B9	32 00 28
	02BE	LD A 0A	7	02BC	3E 0A
	02C1	LD (2800) A	13	02BE	32 00 28
	02C2	DEC HL	6	02C1	2B
	02C3	DEC D	4	02C2	15
	02C4	LD A D	4	02C3	7A
	02C7	LD (27FE) A	13	02C4	32 FE 27
	02C9	CP 00	7	02C7	FE 00
	02CB	JR Z 02	7/12	02C9	28 02
	02CD	JP (IX)	8	02CB	DD E9
	02CF	LD A 30	7	02CD	3E 30
	02D2	LD (27FE) A	13	02CF	32 FE 27
Return to DATOU	0290	RET	10	02D2	C9

Note 1: Comment on sampling frequency.
Sampling Period, T = {18X + 20}Y + 8,
where X=value in register C,
and y=value in register B.

Note 2: Comment on waiting duration.
Wait Duration, D = {{18X + 13}12Y + 13}12Z +7,
where X=value in register E,
Y=value in register D,
and Z=value in register C.
[Both times are measured in processor clock cycles].

c. ROM TEXT LISTING.

TEXT	ROM ADD.	ASCII	TEXT	ROM ADD.	ASCII
CR	0700	0D	T	06E0	54
STX	06FF	02	E	06DF	45
D	06FE	44	:	06DE	3A
A	06FD	41	LF	06DD	0A
T	06FC	54	LF	06DC	'0A
E	06FB	45	LF	06DB	0A
:	06FA	3A	LF	06DA	0A
LF	06F9	0A	LF	06D9	0A
LF	06F8	0A	LF	06D8	0A
S	06F7	53	LF	06D7	0A
T	06F6	54	LF	06D6	0A
A	06F5	41	LF	06D5	0A
R	06F4	52	LF	06D4	0A
T	06F3	54	C	06D3	43
-	06F2	2D	H	06D2	48
T	06F1	54	A	06D1	41
I	06F0	49	N	06D0	4E

M	06EF	4D	SP	06CF	20
E	06EE	45	SP	06CE	20
:	06ED	3A	SP	06CD	20
LF	06EC	0A	D	06CC	44
LF	06EB	0A	A	06CB	41
S	06EA	53	T	06CA	54
H	06E9	48	A	06C9	41
I	06E8	49	SP	06C8	20
F	06E7	46	SP	06C7	20
T	06E6	54	SP	06C6	20
:	06E5	3A	U	06C5	55
LF	06E4	0A	N	06C4	4E
LF	06E3	0A	I	06C3	49
N	06E2	4E	T	06C2	54
O	06E1	4F	SP	06C1	20
SP	06C0	20	SP	0673	20
SP	06BF	20	O	0672	4F
C	06BE	43	.	0671	2E
O	06BD	4F	S	0670	53
M	06BC	4D	.	066F	2E
M	06BB	4D	SP	066E	20
E	06BA	45	F	066D	46
N	06B9	4E	A	066C	41
T	06B8	54	I	066B	49
SP	06B7	20	L	066A	4C
SP	06B6	20	E	0669	45
BEL	06B5	20	D	0668	44
LF	06B4	07	.	0667	2E
LF	06B3	0A	ETX	0666	03
ETX	06B2	03	NUL	0665	00
NUL	06B1	00	¦		¦
¦	06B0	¦	¦		¦
NUL	069F	00	NUL	0661	00
STX	0680	02	STX	0660	02
F	067F	46	F	065F	46
A	067E	41	A	065E	41
T	067D	54	T	065D	54
A	067C	41	A	065C	41
L	067B	4C	L	065B	4C
SP	067A	20	SP	065A	20
F	0679	46	F	0659	46
A	0678	41	A	0658	41
U	0677	55	U	0657	55
L	0676	4C	L	0656	4C
T	0675	54	T	0655	54
:	0674	3A	:	0654	3A
			SP	0653	20
			F	0652	46
R	0651	52	SP	0633	20

A	0650	41
M	064F	4D
I	064E	49
N	064D	4E
G	064C	47
SP	064B	20
F	064A	46
A	0649	41
I	0648	49
L	0647	4C
E	0646	45
D	0645	44
.	0644	2E
ETX	0643	03
NUL	0642	00
NUL	0641	00
STX	0640	02
F	063F	46
A	063E	41
T	063D	54
A	063C	41
L	063B	41
SP	063A	4C
F	0639	20
A	0638	46
U	0637	41
L	0636	55
T	0635	4C
:	0634	54

A	0632	41
L	0631	4C
G	0630	47
O	062F	4F
R	062E	52
I	062D	49
T	062C	54
H	062B	41
M	062A	4F
SP	0629	54
N	0628	20
O	0627	4F
T	0626	54
SP	0625	20
F	0624	46
O	0623	4F
U	0622	55
N	0621	4E
D	0620	4F
.	061F	2E
ETX	061E	03
NUL	061D	00
NUL	061C	00

CHAPTER 8

SYSTEM INTEGRATION

In this closing chapter we examine the problem of getting the diverse parts of the D.A.S. to work together (integration). This includes commissioning procedures and measured D.A.S. performance. The last two sections are a summary, a set of recommendations primarily intended for CMB Packaging Ltd. technical Managers and a discussion of possible areas of further research related to this project.

8.1 Commissioning Notes.

It is generally accepted that the laboratory performance of a system is not entirely representative of its behaviour under operational conditions. For practical reasons however it is usually meaningful to be able to perform laboratory tests as presented in

this project before an attempt is made to install a system for operational testing. It therefore needs stating that the performance measured in this work is under simulated conditions. Although an attempt has been made to approximate operational conditions of the system inputs, the contribution of environmental factors has not been fully investigated. For this reason, certain issues of functionality, especially calibration were deferred from the analysis to this section because they require to be done on site. This is especially true of the analogue cicuits in the D.A.S. In dealing with commissioning and system integration, we list the various D.A.S. units and the recommended approach to those issues.

(i) Analogue Transmitters (TT-A).

It is useful that during calibration of this unit the manufacturer's data sheets for the AD595AQ IC be available. There are four things to be done in calibrating this unit. These are: correct cold junction compensation (CJC), correct positioning of the zero point, setting of the AD595AQ output voltage

gain and setting the voltage-to-current interfacing into the current loop. Granted that the chosen current loop transmission standard has a current of 10 mA at no-input signal and the current varies linearly between 10-50 mA. Granted also that calibration is desired for 0-250 °C but tuned to perform best between 148 °C and 202 °C. Select the median of 148 °C and 202 °C as the calibrating temperature for off-set purposes. This corresponds to a loop current of 38 mA *i.e* at 175 °C.

Since the AD595AQ is already pre-calibrated for K-type TC's we describe here the recommended procedure for dealing with J-type TC's. Devices referred to are in the TT- A (Fig. 6.1) circuit and "Cropico" is the thermocouple simulator unit used at the CMB site. The procedure is shown in form of the routine chart of Fig. 8.1. A thermometer for ambient temperature measurement and a thermocouple simulator ("Cropico") are required. The numbers in Fig. 8.1 represent the following steps:

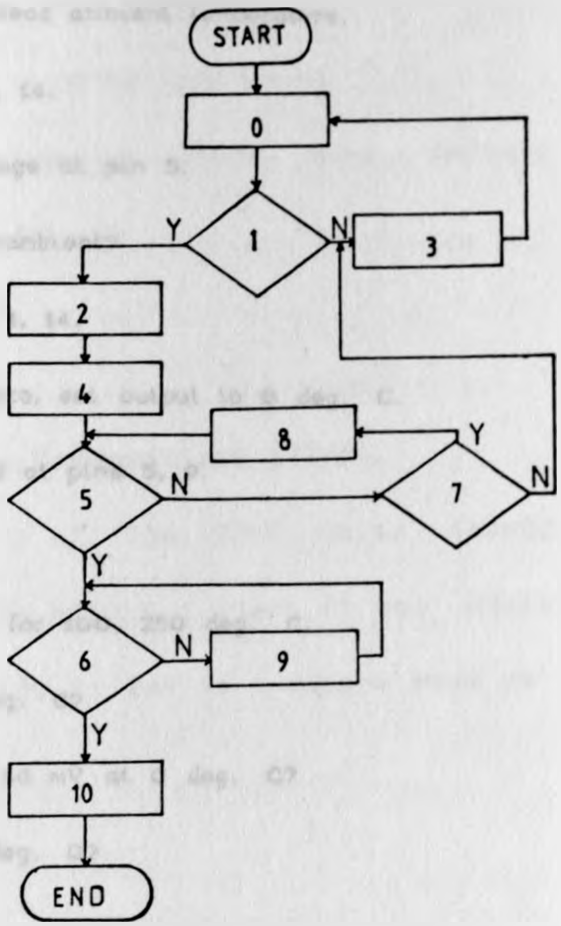


Fig. 8.1 Procedure for calibrating a TT-A.

Calibration of the TT-A

(To be used together with data sheet for the ADQ595AQ and Fig. 8.1. Pin no.s refer to IC 1 on TT-A circuit of Fig. 6.1).

0 : Power "ON". Read ambient temperature.

Short pins 1, 14.

Measure voltage at pin 5.

1 : Pin 5 voltage=ambient?

2 : Separate pins 1, 14.

Connect Cropico, set output to 0 deg. C.

Read voltages at pins 5, 9.

3 : Adjust R2.

4 : Repeat step 2 for 100, 250 deg. C.

5 : Gain=40 mV/deg. C?

6 : TP1 voltage=8.56 mV at 0 deg. C?

7 : CJC=51.5 μV/deg. C?

8 : Adjust R8.

9 : Adjust R3.

10: Set Cropico to 175 deg. C.

Adjust R5 to Loop current=38 mA.

11: END OF PROCEDURE.

TT-A is calibrated for:

TC-J-type

TP1 voltage=(type J voltage (refd. to 0 deg. C)

+zero off-set) X 776.4.

Voltage gain=40 mV/deg. C.

Calibration range: 0-250 deg. C,

10-50 mA Loop current,

Linearity (zero) error centering at 175 deg. C.

(ii) Pulse Transmitters (TT-P).

The accuracy of the TT-P units depends on the efficacy of the strict filter. It was explained that the input to the filter is a square wave as shown in Fig. 8.2.

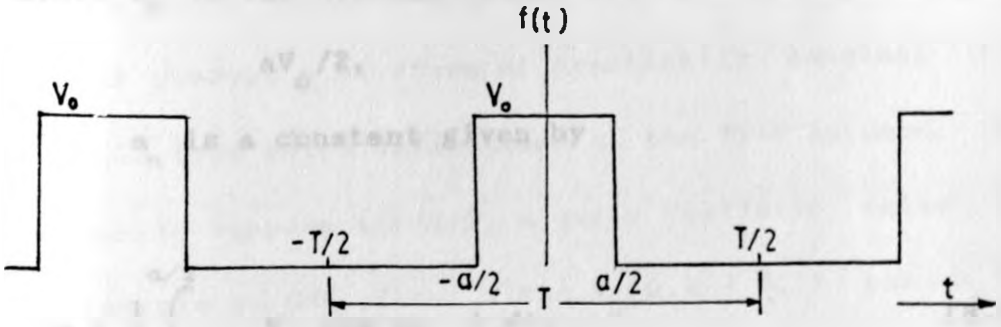


Fig. 8.2 Graphical representation of counter pulses.

Since the precise values of the filter are highly

dependent and specific to the application an analytical exposition of the working principles is possibly of greatest help here.

Assume that the counting head senses objects of the same length and roughly passing at the same rate during normal operation. Then the periodic waveform of Fig. 8.2 is valid. According to *Fourier* theory, [28] the square wave time signal can be expressed in terms of its frequency components as

$$f(t) = a_o + \sum_{n=1}^{\infty} a_n \cos nw_o t \qquad (8.1)$$

where a_o is the average value of the waveform *i.e.*

$$aV_o/2,$$

a_n is a constant given by

$$a_n = \frac{1}{T}\int_{-a/2}^{a/2} V_o \cos n\omega_o t \, dt, \qquad (8.2)$$

and $\omega_o = 2\pi/T$.

From eqns. (8.1) and (8.2), the waveform out of the TT-P is given by

$$f_T(t) = aV_o/T + 2V_o/2\pi \sin(a\omega_o/2)\cos \omega_o t. \quad (8.3)$$

We have assumed that the strict filter in the TT-P has been applied to eqn. (8.1) such that only frequencies below n=1 pass out of the TT-P.

It is seen that the resulting waveform has a d.c. component and an oscillatory value whose amplitudes are a function of the duty cycle. Information carried by the waveform of eqn. (8.3) is both in the d.c. value (from which the duty cycle can be obtained) and also in the oscillation (from which the period of the square wave can be obtained if duty cycle is known). In general actual production lines in normal operation will produce a waveform of practically constant duty cycle from which calibration of the TT-P is done. For example suppose a/T=0.8, a quite realistic value for tinplate at CMB. Then $f(t)= V_o\{0.8 + 0.37 \cos \omega_o t\}$. An application routine at the receiver then reads several values of the TT-P and determines the minimum and maximum values.

From this it is able to obtain the period of the

received waveform and hence the sensor counting rate. In this case it is not necessary that a/T be known but simply that it be constant so that the amplitude of cos $\omega_o t$ be also constant.

Alternatively if the duty cycle for each production item is known the application routine can instead use the term with sin $(a\omega_o/2)$ to relate the amplitude of the received waveform to the source frequency. The attraction for this kind of algorithm is that it does away with real timing and may use a look-up table relating the product being counted to the duty cycle a/T. The relationship between counting frequency and the oscillatory signal peak to peak loop current for the filter shown in the prototype TT-P unit is shown in Fig. 6.3.

Clearly the filter specification and calibration procedures are particular to the specific counting situation even though their design should be in line with the explanation above. The gain of the filter must for example, together with R15 ensure that the output signal in the loop is less than 50mA peak to peak. It is also seen that (Fig.6.3) the sharpness of

the filter will affect accuracy and linearization.

(iii) Concentrator Unit-Driver Board.

On this board, there are three points to be considered. The first is that all current loop input signals should be low-pass filtered at 1.7 Hz. This eliminates noise picked up outside the signal band for oven monitoring channels. (Recall that counting channels are bandlimited to about 1.7 Hz and temperature channels far below). Consequently since sampling is in fact at 25 Hz, the spectra of the sampled signals are separated by at least 20 Hz. By implication a single pole anti-aliasing filter used with these channels affords at least 12dB attenuation of aliasing spectra. Thus simple RC filters are used at the multiplexer inputs with their 3dB points at 1.7 Hz. The important point here as related to commissioning is that monitoring channels of another bandwidth will require re-evaluation of these filters.

The second point relates to the framing pattern. This pattern is generated by using a potentiometer connected across the regulated power supply. The

variable resistance supplies a variable voltage to channel 0 of the multiplexer. Suppose it has been decided that the framing pattern is F5 H. This is the digital output desired at the A/D converter. Since the converter reference voltage is 2.5V, representing FF H, then F5 corresponds to 2.4V. This potentiometer is thus set nominally to 2.4V. Then the multiplexer clock is disabled and channel 0 selected such that only this analogue input corresponding to the framing pattern is digitised. The output of the A/D converter is monitored and the 2.4V finely adjusted to produce the framing pattern. The choice of the framing pattern should correspond to a data value that is unlikely to arise from analog inputs during normal system operation. For example F5 H is chosen because it corresponds to a temperature of 245 $^{\circ}$C in the ovens. This cannot normally be achieved because oven over-temperature watchdog circuits at CMB will shut down the ovens beyond about 225 $^{\circ}$C.

The third point relates to calibration of the Unit for operation with the CL front end. To calibrate these input channels the voltage generated by a signal

current across a known resistance is measured. The process then proceeds along the following lines. Set the current in TT loop to 50 mA. Fine-adjust the sensing resistor on the C.U.-Driver Board so that the input to the comparator is exactly 2.5V. This resistor is nominally 50Ω. (If very high precision is desired it is recommended that a four terminal wire-wound fixed resistor be used instead). With this arrangement 50 mA of signal current will correspond to a digitised value of FF H.

(iv) Concentrator Unit - Data Board.

On this board R1 can be adjusted to attenuate equally all signals from the multiplexer. This may be useful if a scaling factor is required for some reason. R6 is used to correct offsets on the LM311 comparator and C4 may be used to fine-tune the master clock frequency. If clocking is to be adjusted, then it is best to monitor the high frequency clock and set it as accurately as possible. This gives higher accuracy for the lower frequencies. Under normal circumstances R1 should be set to zero before programming the framing pattern.

(v) User-end Data Terminal (U.D.T.).

Proper commissioning of this unit requires that the operator settings be correct for the installed software. For the prototype, the required values are those shown in Table 7.1. The unit should be switched "ON" and left for at least 1 minute before the RESET button is pushed to commence proper operation.

(vi) The Integrated System (complete D.A.S.).

It can be seen from above that it is possible to calibrate each composite unit separately. The design specifications are for modularly interchangeable units. The important benchmarks for system integration are:

. Ensure that the TT units modulate the loop current over 10-50 mA over the dynamic range of the monitored variable.

. Ensure that the input filters to the multiplexer are compatible with anti-aliasing requirements for each input channel.

. Program the framing pattern by reading actual digital data at the A/D converter output.

- Note that the A/D conversion returns a value of FF H for an analogue input signal of +2.5V.
- Use R1 on the C.U.-Data Board to apply global scaling to all input channels (including the framing pattern).
- Note that a 1 minute set-up time is recommended after power "ON" for the U.D.T.
- U.D.T. output is valid only when properly initialised by the RESET button after power "ON" and when the "FRAMED" light is "OFF".
- Data from the installed output routine, DATOU, is in hexadecimal.
- The UART output transmission parameters are given in Table 6.1. LK1 and 2 (U.D.T.) give transmission options of 600 and 300 bits per second respectively.
- It is occasionally possible for the system software programs to be derailed; (presumed due to noise). This is especially critical during the system initialization and frame acquisition phase when no error can be tolerated at all in program execution. So if the system appears to take too

long (exceeding 5 minutes) to indicate framing success and make the first print-out, it is recommended to RESET it. However if left alone, the system appears to invariably find its way and regular operation starts within about 10 minutes. (Though the real reason for this ability is not clear, it is suspected that the program ultimately encounters an instruction which resets the program counter to the cold start). It may also be stated that no signs have been noted that after the system is able to make the first valid output down-loading, it can later derail. This is not to suggest that data can not be corrupted by noise but rather that once the system has entered the application programs, errors are not fatal to operation continuation.

8.2 Performance, Limitations and Cost.

In preceding discussions, the design expectations and measured performance have been described side by side. This has been in an attempt to clarify both the design concepts and the behaviour of the realised

system. However, it is intended to bring together in this section an overall insight into the performance and limitations of the realised system. This is particularly aimed at exposing the following:

. Practical problems related to design, implementation and testing.

. More performance data.

. Limitations of the conclusions from the tests.

. Cost factors.

. Other possible applications of the prototype.

The objective here is to give in a nutshell an indication of the kind of the level of performance and problems one wishing to develop this prototype into a production model of the D.A.S. may expect.

(a) Practical problems of design, implementation and testing.

In the ideal design and development environment, there needs to be at least specific subject literature, quick prototyping systems and laboratory testing equipment. In recent times computer aided

design often avails simulation capability in software before prototyping. (Prototyping in this case implying the construction of a scale physical model of the product). In any case quick prototyping facilities for electronics circuits is crucial to quick product development at low cost.

In this case several serious limitations were encountered :

. The only printed circuit board (pcb) design software package available (smARTWORK) was found rather weak in designing any but the simple TT circuits. This not only cost a great deal in time designing the layout, it also led to extensive re-touch work after etching.

. Even with camera-ready artwork, finding a studio with adequate facilities was not easy. Getting good artwork positives at the right scale for the fine tolerance of the IC's was particularly difficult. It calls for a camera precision not readily found.

. Testing of the prototype was limited to some extent by unavailability of at least four useful pieces of test equipment. These are:

(i) noise generator,

(ii) impulse generator,

(iii) spectrum analyzer, and

(iv) Z80 microprocessor development system.

Though not strictly necessary for testing, an oscilloscope camera would also have been useful for recording of information. The point in listing these is to draw attention to some of the factors to be taken into account if one is to do further research or development work on this topic. In particular any attempt to further develop the D.A.S. must not underestimate their significance.

(b) Specific module performances and limitations.

Information in this Section complements that in Chapter 6 but with special emphasis on system limitations. The accompanying graphs are considered essentially self-explanatory and their interpretation is not developed in the text.

1. TT-A Modules.

The current loop transmission system resolution assumes a maximum operating temperature of 250 °C. If operating temperatures exceeding this are in use, this unit may have to be re-designed. In particular, if J or K thermocouples are used the the AD595AQ amplifier may still be used but a more rigorous linearization calibration observed. As the dynamic temperature range of the monitored system increases, linearization problems will become more critical as will be seen from Fig. 3.2. There is a second limitation of this unit. The AD595AQ is specifically designed to suit types K and T thermocoules. Systems requiring use of other types of thermocouples may require that the unit be re-designed. An alternative to re-designing is to consider purchasing standard thermocouple transmitters available on the open-market if cost and performance factors allow. Figures 8.3 show more performance curves for this module.

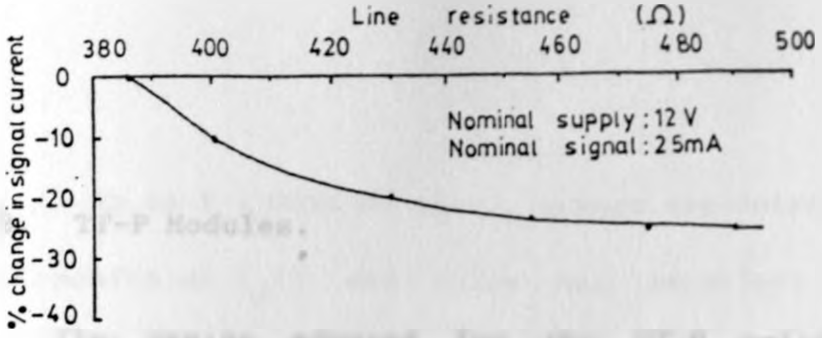


Fig. 8.3a Effect of Loop resistance on signal current from a TT-A.

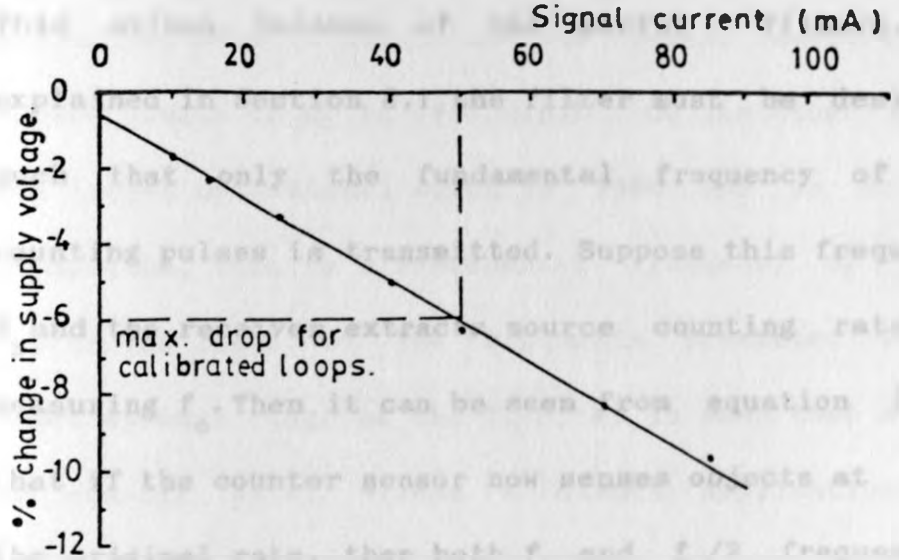


Fig. 8.3b Drop in TT-A supply with signal current.

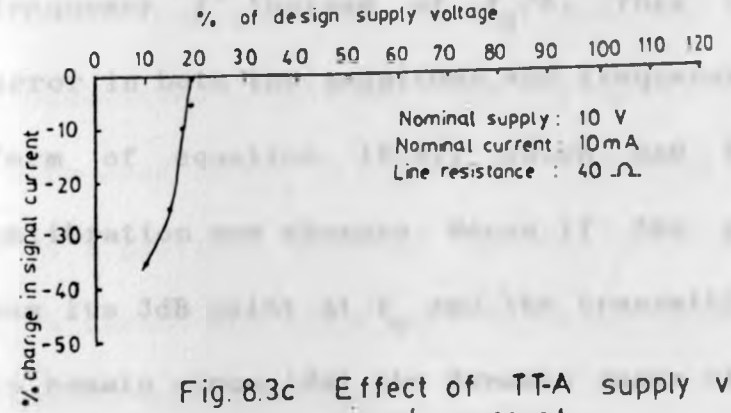


Fig. 8.3c Effect of TT-A supply voltage signal current.

2. TT-P Modules.

The design adopted for the TT-P units while allowing for simplicity, ruggedness and low cost, imposes a somewhat rigid limit on their dynamic range. This arises because of the strict filters. As explained in Section 8.1 the filter must be designed such that only the fundamental frequency of the counting pulses is transmitted. Suppose this frequency f_o and the receiver extracts source counting rate by measuring f_o. Then it can be seen from equation (8.3) that if the counter sensor now senses objects at half the original rate, then both f_o and $f_o/2$ frequencies will pass through the filter. The receiver thus sees the combination of these two waveforms and extracts source counting rate from the resultant waveform of frequency f' instead of $f_o/2$. This introduces an error in both the magnitude and frequency because the form of equation (8.3), which had been used in calibration now changes. Hence if the strict filter has its 3dB point at f_o and the transmitted signal is to remain sinusoidal the dynamic range of the TT-P must be limited to counting rates between just above

$f_o/2$ up to f_o. Outside these, errors are introduced by harmonics at $f_o/2$ and below and imperfect lowpass filtering which allows values greater than f_o.

For example the TT-P designed has its 3dB point at 1.3 Hz because in practice ovens do not exceed 4500 sheets per hour (s.p.h.). So the system calibration allows counts of up to 4680 s.p.h.. On the other hand the lowest operational speed is 3500 sph in normal production. This is a fundamental frequency of 0.97 Hz. In the light of the arguments presented above about dynamic range of the TT-P, it is seen that a 1.3 Hz cut-off point allows a direct application of equation (8.4). Thus the filter in the TT-P is appropriate for operation without concern for dynamic range errors for $0.65 < f_o \leq 1.3$ Hz. In other words within the normal operating range of the ovens. However outside this range counting accuracy is progressively impaired. With a stricter filter, errors introduced by $nf_o > 1.3$ can be virtually eliminated; (n is a positive integer). However those due to $f_o \leq 0.65$ cannot and would have to be corrected for in the receiver calculations.

One way round this problem is to obtain empirical data of the form of Fig. 6.3 and store it as a look up table in ROM. Thus all the Processor need do is read the current output of a TT-P loop and then read off the corresponding count. This is only necessary if counting rate must be strictly accurate outside one octave. Above these extra limitations the TT-P behaves much like the TT-A (Fig. 8.4).

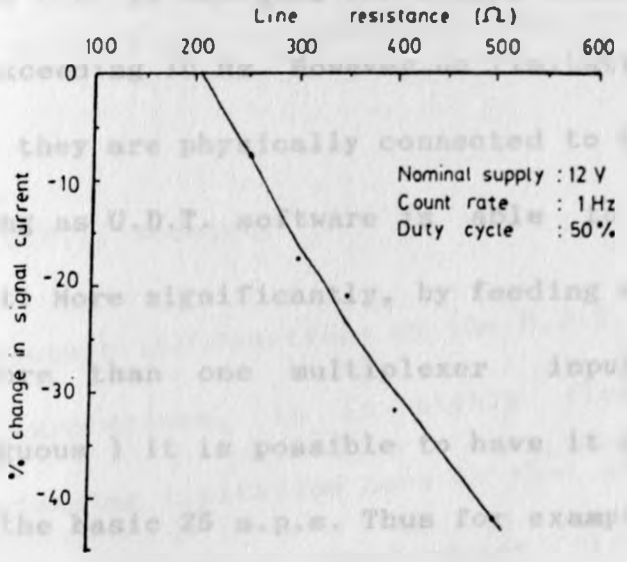


Fig. 8.4 Effect of Loop resistance on signal current from a TT-P.

3. C.U. Modules.

The limitations of this type of module are in the number of input channels, the type of input signals, its bandwidth and A/D conversion resolution and accuracy. The signal channels are limited to 47 and are all required to be of the current loop transmission standard. The specific (0-20, 4-20, 0-50 or 10-50 mA) standard is not a serious limitation because inter-conversion is straight forward.

The C.U. is designed for single channel bandwidths not exceeding 10 Hz. However no limitation is put on where they are physically connected to the multiplexer so long as U.D.T. software is able to identify the layout. More significantly, by feeding an input signal to more than one multiplexer input (physically contiguous) it is possible to have it sampled faster that the basic 25 s.p.s. Thus for example if all 48 channels are connected to one input, it will be sampled at 1200 Hz. This means that this single signal can have a bandwidth of up to 480 Hz and meet the same criteria set for 48 x 10 Hz channels. Thus the C.U. is effectively reconfigurable for baseband frequencies

and not limited to signals of the same bandwidth.

A/D conversion resolution is limited to 1/255. The implication of this to system performance is completely dependent on the resolution required in the analogue signal. This may be important if it is desired that data at the receiver be reconstructed into analogue signals. Similar limitations are imposed on the maximum level of the analogue input signal by the use of a 2.5V reference signal in the A/D conversion. It is noted also that clocking ratios are also quite rigid and cannot be easily changed (Fig. 6.5).

4. U.D.T. Modules.

Because the functions of the U.D.T. are essentially software driven, it is highly flexible. The most outstanding limitation here is that imposed by the use of memory mapped input/output (I/O). This places penalties in the significant amount of unusable memory addressing capability sacrificed and in increased execution time of the Processor I/O. The latter arises because special high speed I/O instructions available

in the Z80 are not used. Another point is that the fact that memory is not fully decoded may be found to be a critical factor in limiting system expansion. Effectively the system is limited to a maximum memory of 8 Kbytes unless a different approach to memory management is taken. The acceptability of this compromise is dependent on the requisite data processing power of the D.A.S. If the current memory arrangement is found unacceptable one option would be to install a memory management expansion board and relevant code in the U.D.T. This need not disrupt the existing set up nor require extensive redesign.

5. Overall System.

The D.A.S. prototype shows better accuracy performance for normal operation than required by the design criterion of Section 3.1 *i.e.* that of 2.5% full range error. Measured performance shows a D.A.S. acccuracy that exactly meets the stricter transient condition monitoring requirements specified in Section 3.2 and Chapter 5. Overall D.A.S. performance is

summarised in Fig.8.5 in which the analogue inputs to the D.A.S. are compared to the digital data in the U.D.T., the system's output.

(c) On the conclusiveness of the test results.

Test curves have been presented during previous discussions. Here we wish only to point out what we consider the central conclusions and limitations from these tests.

. It is clear from the test data presented that the results are in agreement with theoretical principles as applied to the design of the various units. Thus it was possible to show that the TT units modulated the current in a loop in proportion to the input signal. Also that channel multiplexing could be effected and A/D conversion implemented. Similarly it was shown that digital transmission and reception was feasible. Finally that captured raw analogue data can be recovered after transmission and displayed on the computer-compatible Logic Analyser connected to the U.D.T.

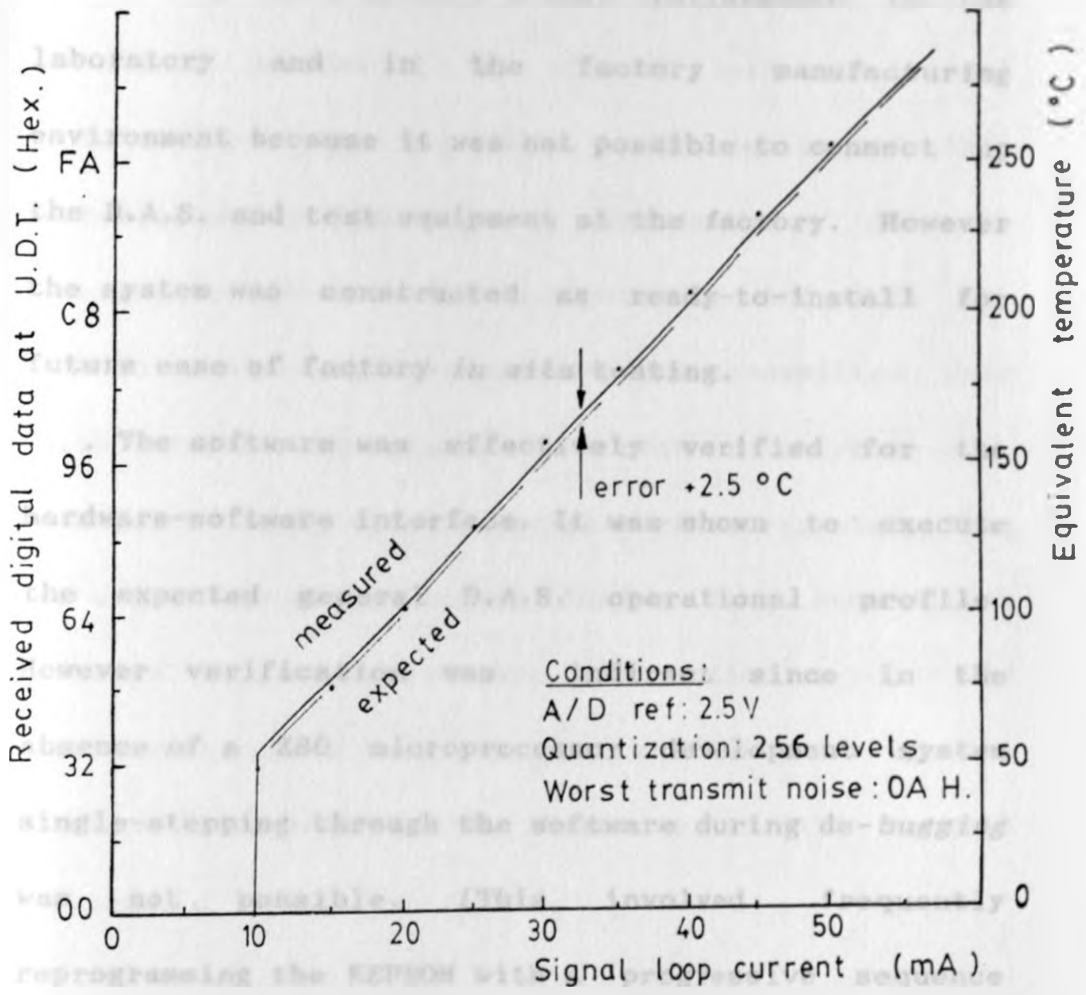


Fig. 8.5 Overall D.A.S. performance.

. No conclusive data was obtained to enable the direct comparison between D.A.S. performance in the laboratory and in the factory manufacturing environment because it was not possible to connect up the D.A.S. and test equipment at the factory. However the system was constructed as ready-to-install for future ease of factory *in situ* testing.

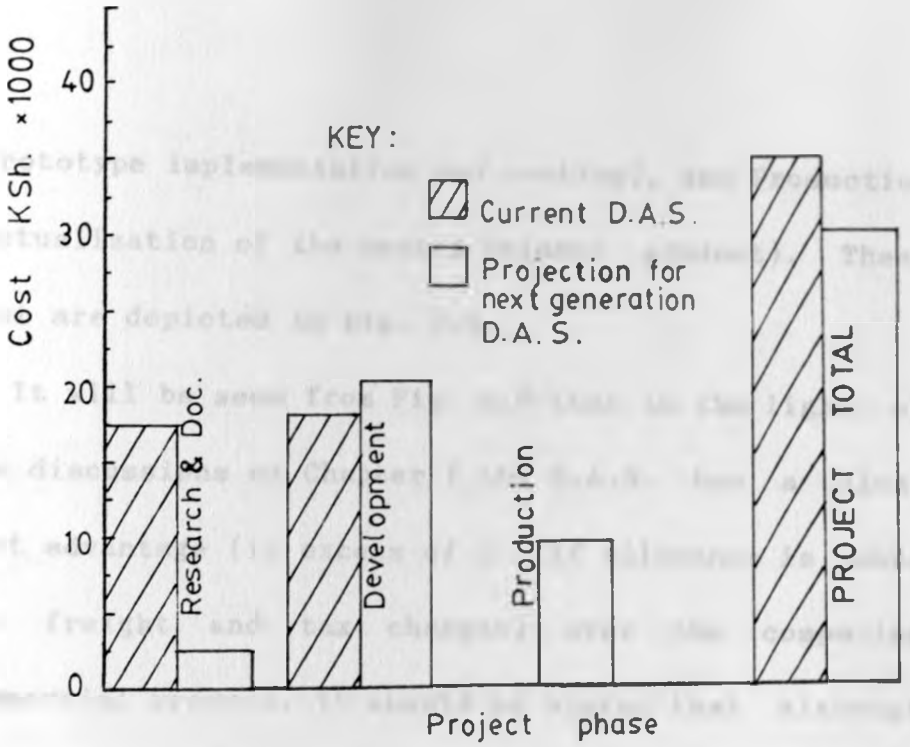
. The software was effectively verified for the hardware-software interface. It was shown to execute the expected general D.A.S. operational profile. However verification was indirect since in the absence of a Z80 microprocessor development system single-stepping through the software during de-*bugging* was not possible. (This involved frequently reprogramming the EEPROM with a progressive sequence of HALT instructions until the expected execution profile was achieved). As such it can not be fairly claimed that the software is conclusively error-free.

. Unavailability of an appropriate RS 232C receiver meant that operation of the D.A.S. with an RS 232C peripheral could not be conclusively verified with hard copy print-out. Thus although the output data

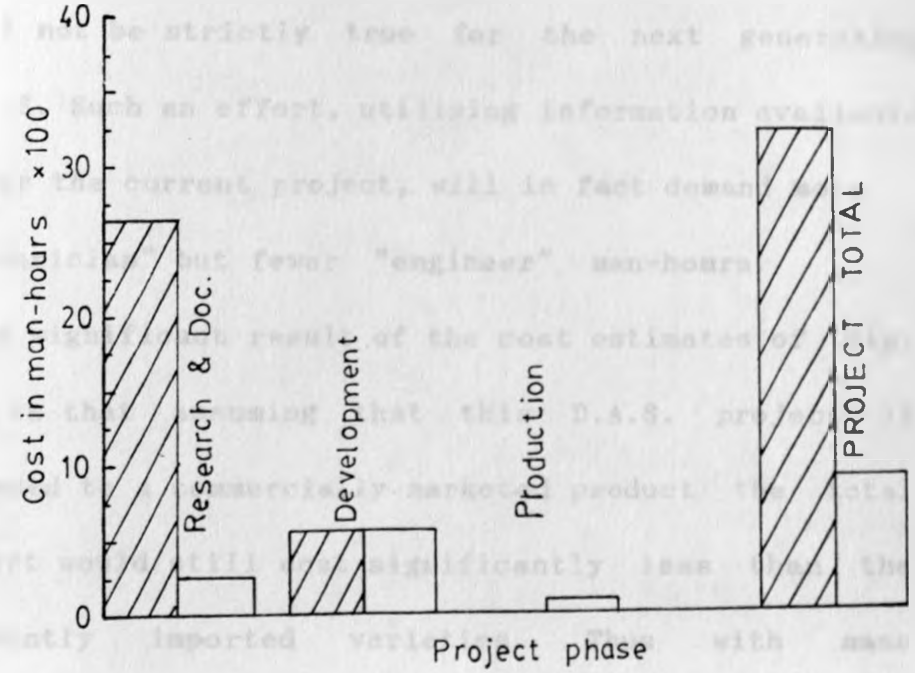
(after processing by the Z80 in the U.D.T.) can be seen on the oscilloscope it is not possible to analyse in detail. However it has already been shown that acquisition of the raw data, transmission of this intelligence and the maintenance of a transmitter-receiver link are possible. And since the U.D.T. receive-register receives the transmitted data with integrity the problem then rests in showing that the U.D.T. application programs work as expected. This is a data processing rather than a data acquisition problem. It is believed that this particular point is not a serious limitation to the conclusiveness of the current functioning of the hardware or the overall system.

(d) Cost.

We now indicate the method by which the D.A.S. project costing was done. The costs are broken down into materials and time. The work itself is divided into logical though not necessarily sequential phases. These are: Research and Documentation, Development



(a) D.A.S. project costs in cash for materials.



(b) Project costs in skilled labour.

Fig. 8.6 Critical D.A.S. cost estimates.

(prototype implementation and testing), and Production (actualization of the market trimmed product). These cost are depicted in Fig. 8.6.

It will be seen from Fig. 8.6 that in the light of the discussions of Chapter 1 the D.A.S. has a clear cost advantage (in excess of 2:1 if allowance is made for freight and tax charges) over the competing commercial product. It should be stated that although the time costing assumes a level of skill equal to that required for this current prototype D.A.S., this will not be strictly true for the next generation D.A.S. Such an effort, utilising information available after the current project, will in fact demand more "technician" but fewer "engineer" man-hours.

A significant result of the cost estimates of Fig. 8.6 is that assuming that this D.A.S. project is pursued to a commercially marketed product the total effort would still cost significantly less than the currently imported varieties. Thus with mass production the D.A.S. would appear to be an extremely attractive offer for most needs.

In Fig. 8.7 we show a photograph of the complete D.A.S. The TT's are on the extreme left hand side. The boards in the middle are the C.U. and the U.D.T. is on the extreme right. Behind each unit are shown respective temporary packing boxes to give a perspective of physical size of an operational unit. The oscilloscope and Logic Analyser represent the system end (data) user in the photograph.

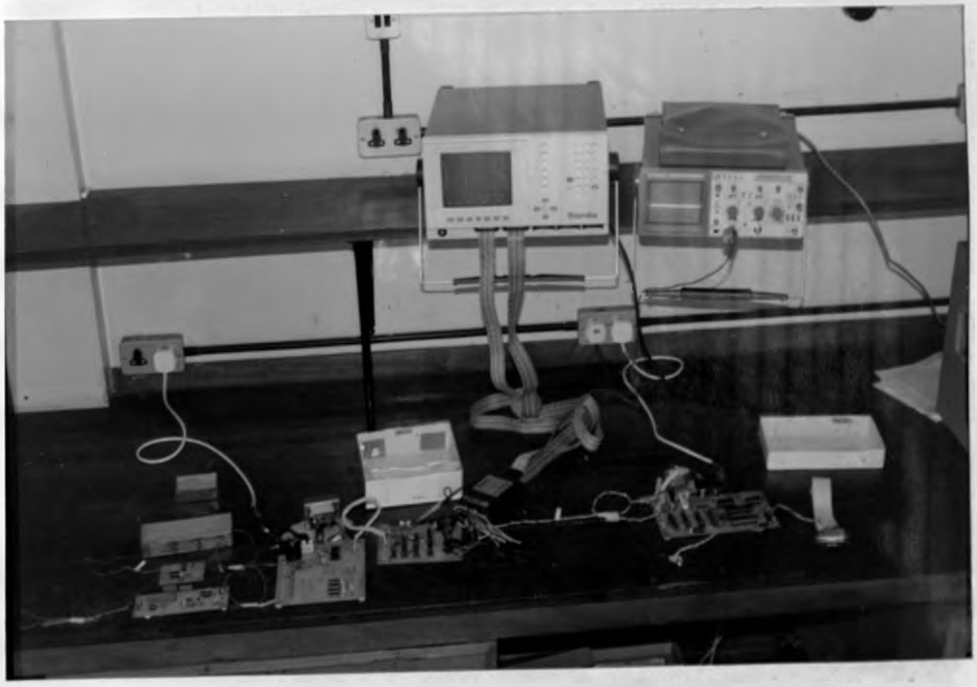


Fig. 8.7 Photograph of the complete D.A.S.

8.3 Summary, Recommendations and Conclusion.

(a) Summary.

An analytical methodology was developed to deal with the problem of process data acquisition in industry. A case study was done to illustrate its application to a medium scale manufacturing plant in Kenya. In particular it was demonstrated that the problem of dealing with factory data aught to be approached systematically. An approach was shown on how to arrive at the specification of a data acquisition system. The specification is believed to be equally applicable to system modules acquired commercially or customer-designed on site.

A prototype data acquisition system (the D.A.S.) was proposed, realised and implemented with special reference to the general needs of the CMB Packaging Ltd. factory in Thika and its Printing Department in particular. It was shown that the prototype is feasible both technically and economically. The D.A.S. prototype was shown to exceed design requirements in

accuracy. Cost comparisons give the prototype a cost advantage of at least 2:1 over commercially competing products. A discussion of its commissioning and performance limitations included in this Thesis will enable its installation for long term operational testing on site. Results of laboratory tests on the system suggest that the D.A.S. concept has excellent potential for development for research or commercial exploitation.

(b) Recommendations.

These recommendations are made essentially for consideration by CMB Packaging Ltd. Management. They result from this study of the data acquisition problem at the CMB Printing department. Though their essence is directly related to the D.A.S. project their overall impact is far broader. They are made in the light of recent trends by the Company towards new manufacturing approaches such as use of high technology and *Total Quality*.

The recommendations are that :

1. The information in Parts I and II of this report form the basis for specifying the data acquisition system for the Printing department.
2. Management consider setting out a comprehensive strategic guideline for the collection, distribution and use of information factorywide *i.e.* formulate a factory wide information policy.
3. The Company plan to purchase essential design and test tools for microprocessor based systems. These are necessary to sustain technology now being installed at the factory and to enhance the Company's design and development capability. The latter is vital in taking advantage of findings such as those of this project.
4. Management seriously consider instructing the Projects Department to investigate the possibility of continuing with this project through development to production.
5. The Company work to establish formal contact with a University with a view to collaboration in research and development as it moves towards use

of highly sophisticated manufacturing technology. The value of such contact to either party cannot be easily over-estimated.

(c) Conclusion.

The general conclusion is drawn that this project succeeded in demonstrating a practical, systematic and cost-effective approach to the industrial data acquisition problem in the medium scale Kenyan factory. Further, that the designed prototype is a viable basis for research and development into a commercial product.

8.4 Further Work.

Possibility for further work extends both to specific problems related to the further development of the designed system and to its use in different applications. Texts that may be useful for this kind of work are listed in the Bibliography.

a. Further Research and Development of the Prototype.

In this direction at least three areas are open for further work. One is the comprehensive testing and measurement of D.A.S. behaviour in noise and the other environmental factors on site. This will help establish empirical comparison for such factors as the probability of error, long term drift and susceptibility to the physically hostile operational environment.

The other area is software development which may extend to exploration of using the same hardware for "hard real-time" systems in fast production lines. This may find use in optimizing high speed track conveyors in the CMB factory *etc.* Together with this is the introduction of user-friendly software, and software for networking the D.A.S. to similar systems.

A third area, though related to the two above takes the approach of product development rather than research. Thus one may consider the prototype as needing product development and aim to make it a commercial product. This may require refinement in its

characteristics, production process, costing and other keys to commercial appeal.

b. Alternative Applications.

Along this line, one may simply consider the prototype D.A.S. as a research or teaching tool and refine it accordingly. It would find specific use in instrumentation research, in the studies of noise in front-end transmission and sampling and A/D conversion in the concentrator unit. If the U.D.T. is treated purely as a serial data receiver, wide scope exists in the study of digital transmission. On the other hand the U.D.T. may be considered purely as a microprocessor support board around which a multiplicity of systems such as a general-purpose microcomputer can be built. This would make it a basic building block for other industrial, consumer or teaching applications.

It should also be interesting to investigate the possibility of extending the D.A.S. into a supervisory control system able to respond to say alarms. [It would appear that the number of permutations for using

the U.D.T. is perhaps limited only by the fact that commercial products will already exist and it may not be meanigful to duplicate]. Alternatively, one can investigate how the U.D.T. can be modified to fit onto a personal computer motherboard to take advantage of the large amount of commercially available data acquisition software.

END.

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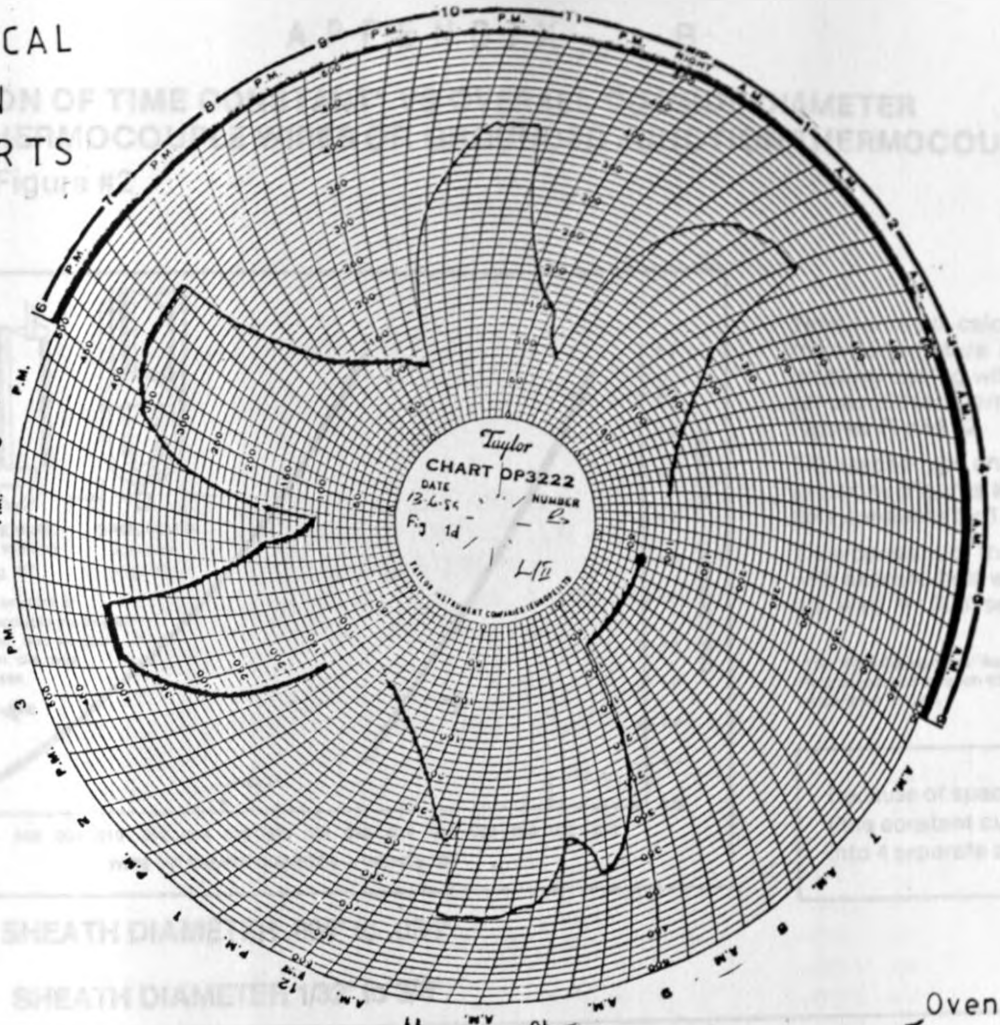
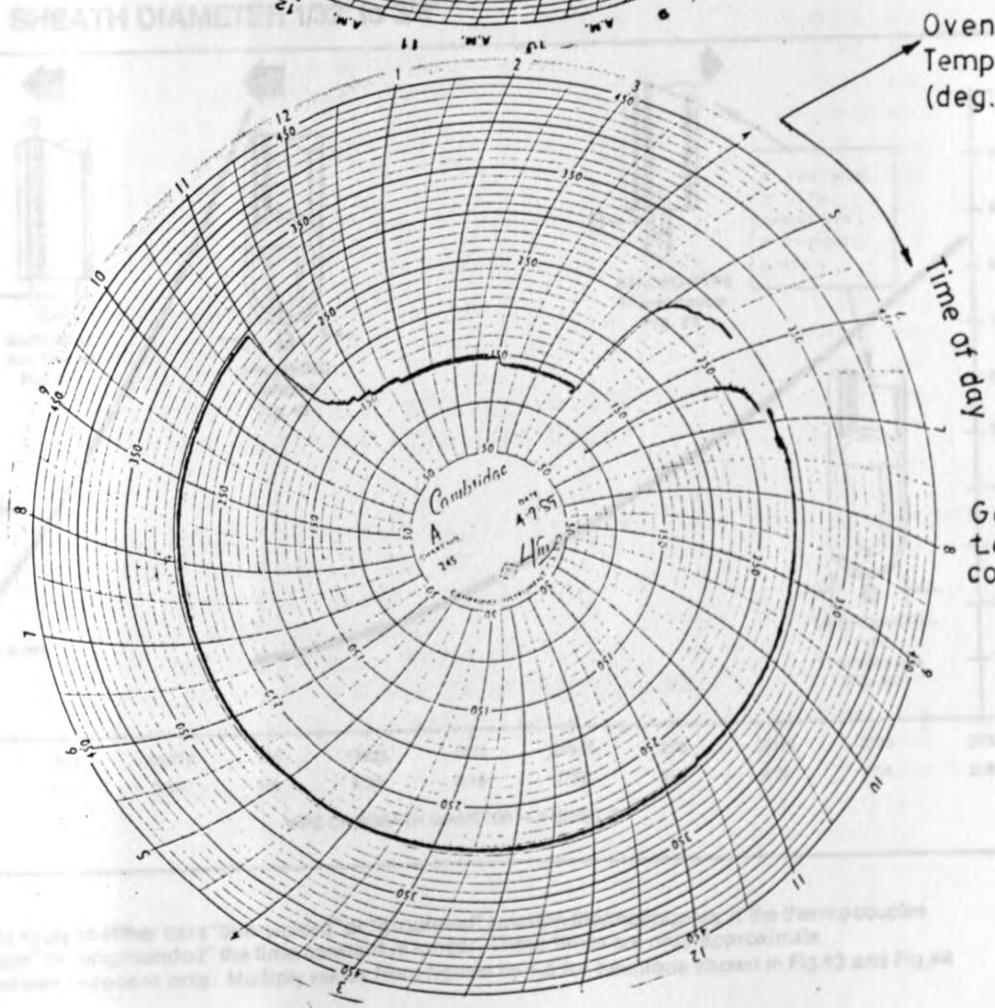
APPENDIX A

TYPICAL OVEN CHARTS



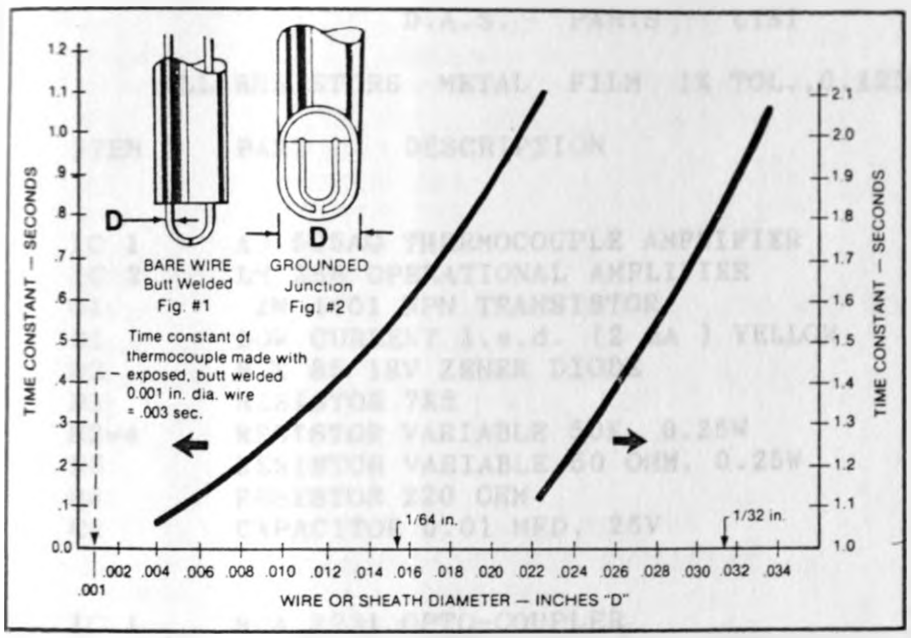
Abnormal condition



APPENDIX B

COMPARISON OF TIME CONSTANT* VS OVERALL OUTSIDE DIAMETER OF BARE THERMOCOUPLE WIRES OR GROUNDED JUNCTION THERMOCOUPLES [29]

Figure #1 & Figure #2



Time constants calculated for air at room temperature and atmospheric pressure moving with velocity of 65 feet per second for thermocouples shown in Figures #1 and #2.

For beaded-type and ungrounded junctions (Figures #3 or #4) multiply time constants by 1.5.

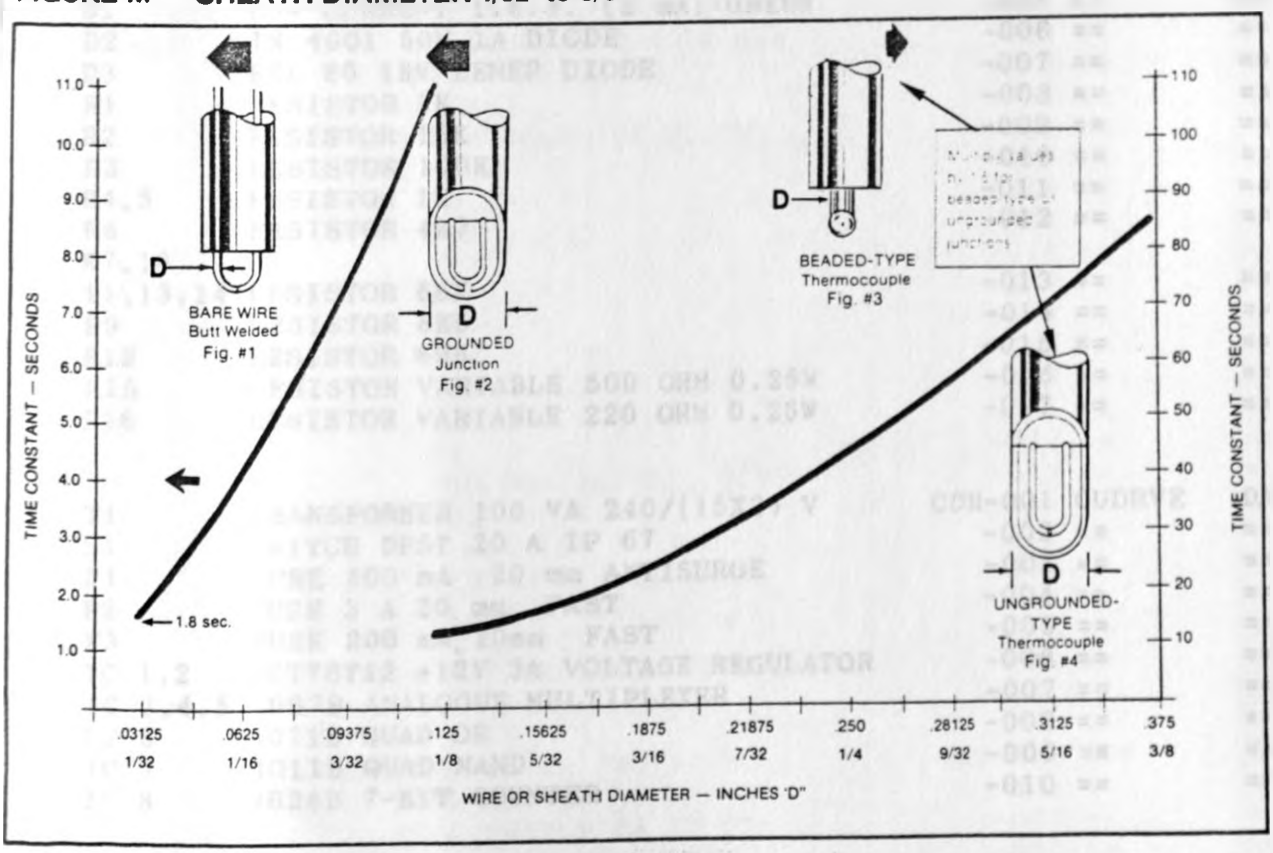
Time constant of thermocouple made with exposed butt welded 0.001 inch dia. wire = .003 sec.

* The "Time Constant" or "Response Time" is defined as the time required to reach 63.2% of an instantaneous temperature change.

Because of space limitations, time constant curve is divided into 4 separate curves.

FIGURE L SHEATH DIAMETER .004" to .034"

FIGURE M SHEATH DIAMETER 1/32" to 3/8"



Note:

These comparisons apply to either bare "butt-welded" or "grounded" junction thermocouples. If the thermo couples are the "beaded-type" or "ungrounded" the time constant is longer. These times are only approximate and are for comparison purposes only. Multiply values from figures by 1.5 for functions shown in Fig.#3 and Fig.#4

APPENDIX C

D.A.S. PARTS LIST

ALL RESISTORS METAL FILM 1% TOL.,0.125W UNLESS OTHERWISE STATED.

ITEM	PART DESCRIPTION	CODE	CCT.	ASSY.DRG.
IC 1	AD 595AQ THERMOCOUPLE AMPLIFIER	TTA-001	TT-A	DAS-01-P
IC 2	LM 358 OPERATIONAL AMPLIFIER	-002	==	==
Q1	2N 4401 NPN TRANSISTOR	-003	==	==
D1	LOW CURRENT l.e.d. (2 mA) YELLOW	-004	==	==
D2	BZX 85 18V ZENER DIODE	-005		
R1	RESISTOR 7K5	-006	==	==
R2-4	RESISTOR VARIABLE 50K, 0.25W	-007	==	==
R5	RESISTOR VARIABLE 50 OHM, 0.25W	-008	==	==
R6	RESISTOR 220 OHM	-009	==	==
C1	CAPACITOR 0.01 MFD, 25V	-010	==	==
IC 1	MCA 2231 OPTO-COUPLER	TTP-001	TT-P	DAS-02-P
IC 2	4093B SCHMITT NAND	-002	==	==
IC 3,4	LM 358 OPERATIONAL AMPLIFIER	-003	==	==
Q1,2	2N 4401 NPN TRANSISTOR	-004	==	==
D1	LOW CURRENT l.e.d. (2 mA) GREEN	-005	==	==
D2	IN 4001 50V 1A DIODE	-006	==	==
D3	BZX 85 18V ZENER DIODE	-007	==	==
R1	RESISTOR 2K	-008	==	==
R2	RESISTOR 15K	-009	==	==
R3	RESISTOR 100K	-010	==	==
R4,5	RESISTOR 1K	-011	==	==
R6	RESISTOR 4K7	-012	==	==
R7,10				
11,13,14	RESISTOR 56K	-013	==	==
R9	RESISTOR 8K5	-014	==	==
R12	RESISTOR 69K	-015	==	==
R15	RESISTOR VARIABLE 500 OHM 0.25W	-016	==	==
R16	RESISTOR VARIABLE 220 OHM 0.25W	-017	==	==
T1	TRANSFORMER 100 VA 240/(15X2) V	CDR-001	CUDRVE	DAS-03-1P
S1	SWITCH DPST 20 A IP 67	-002	==	==
F1	FUSE 400 mA 20 mm ANTISURGE	-003	==	==
F2	FUSE 3 A 20 mm FAST	-004	==	==
F3	FUSE 200 mA 20mm FAST	-005	==	==
IC 1,2	MCT78T12 +12V 3A VOLTAGE REGULATOR	-006	==	==
IC 3,4,5	4067B ANALOGUE MULTIPLEXER	-007	==	==
IC 6	4071B QUAD OR	-008	==	==
IC 7	4011B QUAD NAND	-009	==	==
IC 8	4024B 7-BIT COUNTER	-010	==	==

D1,2	KBU 4D 4A BRIDGE RECTIFIER	-011	==	==
D3,4	l.e.d. (GREEN)	-012	==	==
R1-48	RESISTOR PRECISION 4 TERMINAL 50 OHM	-013	==	==
R49	RESISTOR 100 OHM	-014	==	==
R50	VARISTOR V250 LA4	-015	==	==
R51,52	RESISTOR 4K7	-016	==	==
R53	RESISTOR 33K	-017	==	==
R54,55	RESISTOR 3K3	-018	==	==
R56-104	RESISTOR 91K	-019	==	==
C1,2	CAPACITOR ELECTROLYTIC 10,000 MFD 50	-020	==	==
C3,5	CAPACITOR 330 nF, 16V	-021	==	==
C4,6	CAPACITOR 1 MFD, 16V	-022	==	==
C7	CAPACITOR 0.1 MFD, 16V	-023	==	==
C8	CAPACITOR 0.01 MFD, 1 kV	-024	==	==

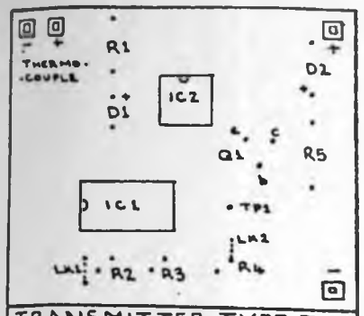
F1	FUSE 200 mA 20mm FAST	CDT-001	CUDATA	DAS-04-2P
IC 1	LM 358 OPERATIONAL AMPLIFIER	-002	==	==
IC 2	LM 311 COMPARATOR	-003	==	==
IC 3	ZN 425E D/A CONVERTER	-004	==	==
IC 4	74LS00 QUAD NAND	-005	==	==
IC 5	78S05 +5V 2A VOLTAGE REGULATOR	-006	==	==
IC 6	4093B QUAD SCHMITT NAND	-007	==	==
IC 7-10	4018B COUNTER	-008	==	==
XTAL1	CRYSTAL OSCILLATOR 2.4576 MHz	-009	==	==
Q1	2N 4401 NPN TRANSISTOR	-010	==	==
D1	l.e.d. (GREEN)	-011	==	==
R1	RESISTOR VARIABLE 10K 0.25W	-012	==	==
R2	RESISTOR 50K	-013	==	==
R3	== 1M	-014	==	==
R4	== 10K	-015	==	==
R5	== 3K3	-016	==	==
R6	== 5K	-017	==	==
R7,8,9,13	== 1K	-018	==	==
R10	== 10M	-019	==	==
R11	== 100K	-020	==	==
R12	== 33K	-021	==	==
R14	== 4K	-022	==	==
R15	== 100 OHM 1% TOL. 0.25W	-023	==	==
C1,3	CAPACITOR 330 nF 16V	-024	==	==
C2	== 1 MFD 16V	-025	==	==
C4	CAPACITOR TRIMMER 5-22 pF	-026	==	==
C5	== 0.1 MFD 16V	-027	==	==
C6	22 pF 16V	-028	==	==
C7	CAPACITOR ELECTROLYTIC 10 MFD 16V	-029	==	==

T1	TRANSFORMER 20 VA 240/7.5V	UDT-001	UDT	DAS-05-P
S1	SWITCH DPST 20A IP 67	-002	==	==
S2	SWITCH PUSH-BUTTON 5A IP 67	-003	==	==
F1	FUSE 50 mA 20mm ANTISURGE	-004	==	==

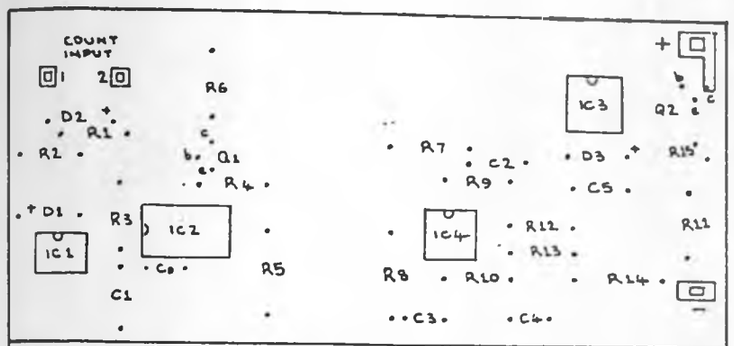
F2	FUSE 630 mA 20 mm FAST	-005	==	==
IC 1	78S05 +5V 2A VOLT REGULATOR	-006	==	==
IC 2	HCPL 2601 HIGH SPEED OPTO-COUPLER	-007	==	==
IC 3	4093B QUAD SCHMITT NAND	-008	==	==
IC 4-7	4018B COUNTER	-009	==	==
IC 8	74LS138 8-TO-1 DECODER	-010	==	==
IC 9	74LS74A D-FLIP-FLOP	-011	==	==
IC 10	Z80 MICROPROCESSOR	-012	==	==
IC 11	2816 2K X 8 BIT EEPROM	-013	==	==
IC 12	6116 2K X 8 BIT RAM	-014	==	==
IC 13	6402 UART	-015	==	==
IC 14	7432 QUAD OR	-016	==	==
IC 15	74LS540 TRI-STATE BUFFER	-017	==	==
IC 16	RS 232C LINE DRIVER	-018	==	==
IC 17	74LS595 8-BIT SHIFT REGISTER	-019	==	==
IC 18	74LS73A JK-FLIP-FLOP	-020	==	==
IC 19	74LS00 QUAD NAND	-021	==	==
D1	KBU 4D 4A BRIDGE RECTIFIER	-022	==	==
D2	l.e.d. (GREEN)	-023	==	==
D3	BZX 85 6V2 ZENER DIODE	-024	==	==
D4	l.e.d. LOW CURRENT (2 mA) YELLOW	-025	==	==
D5	== RED	-026	==	==
D6	IN 4001 50V 1A DIODE	-027	==	==
R1	VARISTOR V250 LA4	-028	==	==
R2	RESISTOR 100 OHM	-029	==	==
R3	== 4K7	-030	==	==
R4	== 500 OHM 1% TOL. 0.25W	-031	==	==
R5	== 3K3	-032	==	==
R6	== 100K	-033	==	==
R7	== 330 OHM	-034	==	==
R8,10	== 33K	-035	==	==
R9	== 10M	-036	==	==
R11	== 2K	-037	==	==
R12	== 7K5	-038	==	==
SIP1	8 X 1K SINGLE-IN-LINE PACKAGE	-039	==	==
C1	CAPACITOR 0.01 MFD 1kV	-040	==	==
C2	CAPACITOR ELECTROLYTIC 10,000 MFD 50	-041	==	==
C3	== 330 nF 16V	-042	==	==
C4	== 1 MFD 16V	-043	==	==
C5	== 22 pF 16V	-044	==	==
C6,8,9	== 0.1 MFD 16V	-045	==	==
C7	CAPACITOR TRIMMER 0-22 pF	-046	==	==

NOTE: ALL ICS' SUPPLIES DECOUPLED WITH 10 nF 16V CAPACITORS.

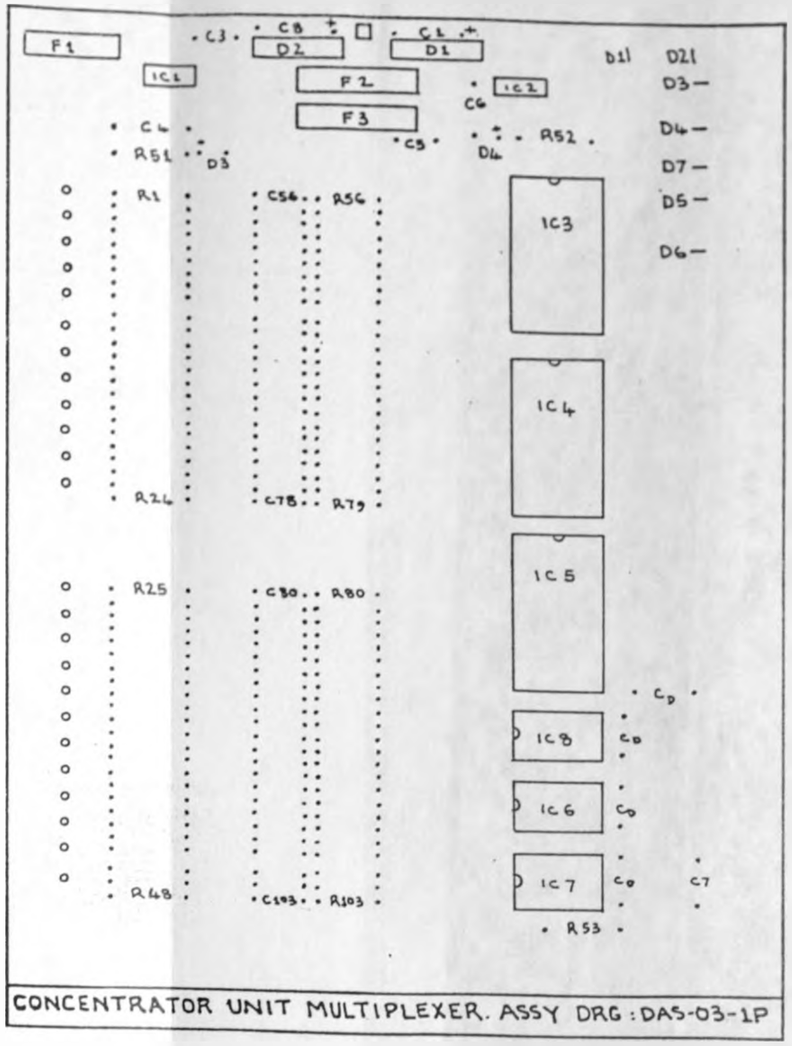
APPENDIX D
D.A.S. ASSEMBLY DRAWINGS



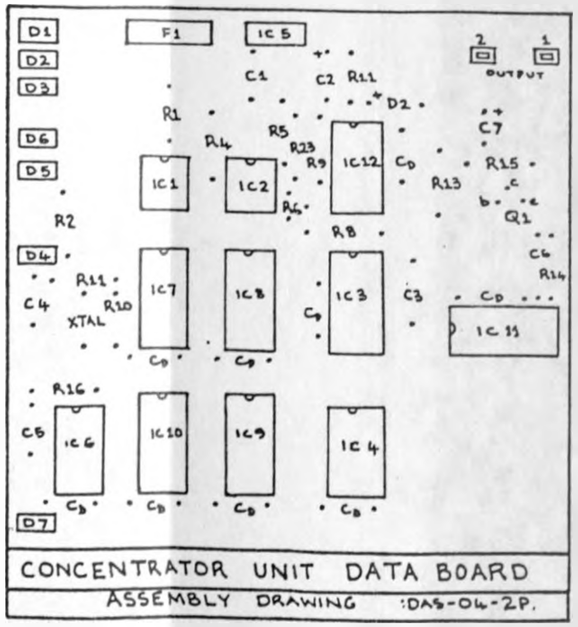
TRANSMITTER TYPE TT-A
ASSY. DRG: DAS-01-P



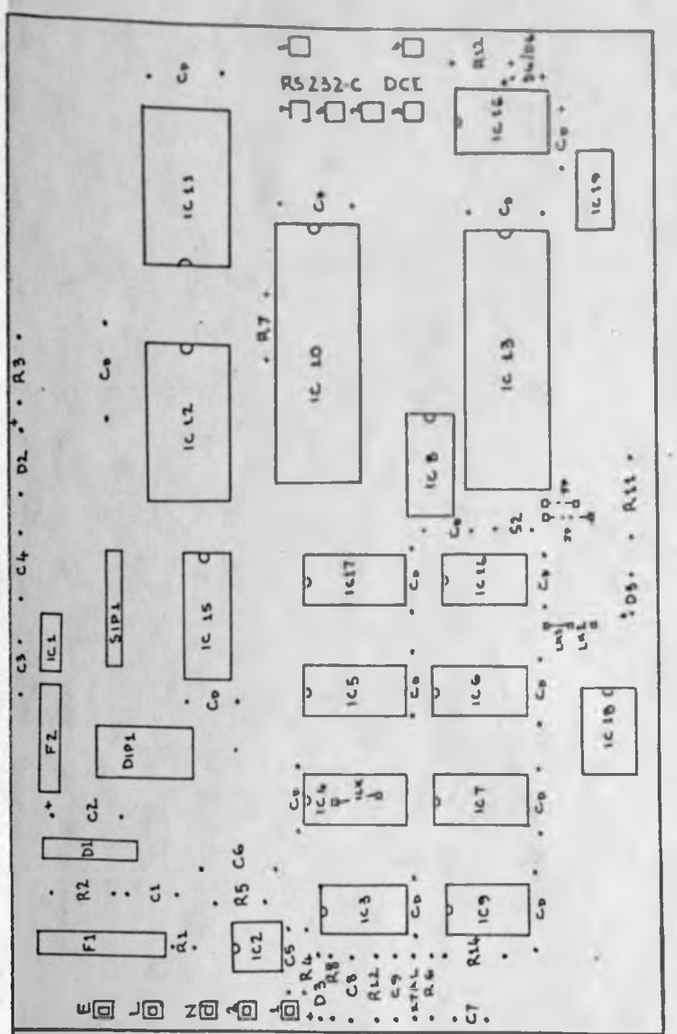
TRANSMITTER TYPE TT-P. ASSY. DRG: DAS-02-P



CONCENTRATOR UNIT MULTIPLEXER. ASSY DRG: DAS-03-1P



CONCENTRATOR UNIT DATA BOARD
ASSEMBLY DRAWING :DAS-04-2P.



USER-END DATA TERMINUS. ASSY. DRG: DAS-05-P.