



UNIVERSITY OF NAIROBI

FACULTY OF ENGINEERING

DEPARTMENT OF ELECTRICAL AND INFORMATION ENGINEERING

DESIGN OF A CARRIER RECOVERY BY REMODULATION IN QPSK

PROJECT NUMBER 66

BY

OTIENO DAVID ACCRA

F17/30085/2009

SUPERVISOR: PROF. V.K. ODUOL

EXAMINER: DR G.S.O. ODHIAMBO

Project report submitted in partial fulfillment of the Requirement the award of the degree

Of:

**BACHELOR OF SCIENCE IN ELECTRICAL AND ELECTRONIC ENGINEERING OF
THE UNIVERSITY OF NAIROBI 2014**

Submitted on: 28th April 2014

DECLARATION OF ORIGINALITY

FACULTY/ SCHOOL/ INSTITUTE: Engineering

DEPARTMENT: Electrical and Information Engineering

COURSE NAME: Bachelor of Science in Electrical & Electronic Engineering

TITLE OF NAME OF STUDENT: OTIENO DAVID ACCRA

REGISTRATION NUMBER: F17/30085/2009

COLLEGE: Architecture and Engineering

WORK:DESIGN OF A CARRIER RECOVERY BY REMODULATION CIRCUITTO BE USED IN QPSK DEMODULATION.

- 1) I declare that this final year project report is my original work and has not been submitted elsewhere for examination, award of a degree or publication.

- 2) I have not allowed, and shall not allow anyone to copy my work with the intention of passing it off as his/her own work.

- 3) I understand that any false claim in respect of this work shall result in disciplinary action, in accordance with University anti-plagiarism policy.

Signature:

Date:

DEDICATION

This project is dedicated to my family especially my father for the support and advice in persuasion of this degree in engineering and my mother for believing in me. Further dedication goes to my uncle Samson OmondiAduda for his commitment towards my education.

ACKNOWLEDGEMENTS

First and foremost, I wish to thank the God for guiding me and being by my side throughout my studies. I would like also to thank my project Supervisor Prof. Vitallice K. Oduol who has always been a guiding factor throughout the project time. It has been a great pleasure for me to get an opportunity to work under him. An assemblage of this nature could never have been attempted without reference to and inspiration from the works of others whose details are mentioned in reference section. I also acknowledge all of them. I also acknowledge all of my friends and classmates who were patiently extended all sorts of help for accomplishing this undertaking.

ABSTRACT

This project aims at designing a carrier recovery circuit based on re-modulation to be used in QPSK demodulator. The circuit can be used in radio frequency range but more specifically the FM range {87MHz to 108MHz}. The idea is based on correcting phase of the received signal. In 1971, Caccianamun and wokjska tried to solve the problem. QPSK is better than BPSK since it is possible to transmit as twice as much information in the same bandwidth and noise relation as in BPSK. Re-modulation is a data aided process and therefore minimal errors occur at the receiver side. The design consists of multipliers, low pass filters, parallel to serial converter, delay, voltage control oscillator, 90^0 phase shifters and limiter.

TABLE OF CONTENTS

Declaration of originality.....	2
Dedication.....	3
Acknowledgement.....	4
Abstract.....	5
CHAPTER ONE: INTRODUCTION	
Background of study.....	8
Statement of problem.....	8
Main objectives.....	9
Specific objectives.....	9
Justification of project.....	9
CHAPTER TWO: LITERATURE REVIEW	
Introduction.....	10
Reasons for carrier extraction.....	10
Methods of carrier recovery.....	10
Limitations of Costas and re-modulator loops.....	11
Advantages of re-modulator loop.....	11
Phase Shift Keying.....	12
Carrier recovery by Costas loop.....	14
Carrier recovery by re-modulation.....	20
CHAPTER THREE: DESIGN OF CARRIER RECOVERY BY REMODULATION IN QPSK	
Design block diagram.....	29
Principle of operation.....	29
Design of circuits that makes the loop.....	30
Implementation of carrier recovery by re-modulation in QPSK in Simulink.....	33
Summary table for block parameters used in the Simulink circuit.....	34

CHAPTER FOUR: RESULTS, DISCUSSION AND ANALYSIS

Results.....35
Discussion.....40
Analysis.....40

CHAPTER FIVE: CONCLUSIONS AND RECOMMENDATIONS

Conclusions.....41
Recommendations.....41

REFERENCES.....42

APPENDIX: glossary.....43

CHAPTER 1

INTRODUCTION

BACKGROUND OF STUDY

Electrical communication is dependable and economical; communication technologies improve productivity and conservation of energy. Increasingly, business meetings are carried out by teleconferencing which saves time used in travelling. It allows real time management and coordination of project participants from around the world. Traditional media outlets such as television, radio and newspapers have been rapidly evolving in the past years to cope with, and better utilize, the new communication and networking technologies. Communication involves implicitly the transmission of information from one point to another through a succession of processes described here[2];

- The generation of a message signal.
- The description of the message signal with a certain measure of precision, by a set of symbols.
- The encoding of this symbols in a form that is suitable for transmission over a physical medium of interest.
- The transmission of the encoded symbols to the desired destination.
- The decoding and reproduction of the original symbols.
- The re-creation of the original message signal, with a definable degradation in quality, the degradation is caused by imperfection in the system.

Communication modes are broadly classified into

- Broadcasting which involves the use of a single powerful transmitter and numerous receivers that are relatively inexpensive to build. Information bearing signals flow only in one direction.
- Point-to-point communication in which the communication process takes place over a link between a single transmitter and a receiver. In this case, there is usually a bidirectional flow of information bearing signal, which require the use of a transmitter and a receiver at each end of the link[2].

STATEMENT OF THE PROBLEM

Transmission of carrier signal wastes transmission power as more power will be required to transmit it. Also at the receiver, demodulation process will not be efficient with the carrier included. Therefore it is necessary to extract carrier signal.

MAIN OBJECTIVE

To study carrier recovery in digital communication systems, and in particular, those based on QPSK and BPSK.

To compare the performance of re-modulation and Costas- based methods for both QPSK and BPSK

To design and demonstrate a carrier recovery by re-modulation for use in QPSK demodulation.

SPECIFIC OBJECTIVES

To design a carrier recovery by re-modulation circuit for use in QPSK demodulation. The main task of the circuit is to extract carrier signal at the receiver.

JUSTIFICATION OF THE PROJECT

Reasons for using QPSK

- In satellite channel the impulse response is zero(no echoes) so we do not need an equalizer for removing intersymbol interference or channel ghosts.
- No specific power requirements.
- Large bandwidth available.
- Signal-to-noise ratio is good.
- Four symbols, and each symbol is two bits, can be transmitted.Carrier recovery by re-modulation in QPSK has faster acquisition time as compared with conventional QPSK Costas loop.

Decision-Directed loops such as re-modulator loop differs from those of Non-Decision Directed loops such as Costas loop and squaring loop only in the way signal amplitude is rectified. In Costas loop each of the two quadrature signals used to correct the signal amplitude is corrupted by noise. In re-modulator loop only one of the signals is corrupted by noise. So decision-directed loop is superior in performance than non-decision directed loop provided that the demodulator is operating at an error rates below 10^{-2} where occasional decision error has a negligible effect on the phase difference[10].

CHAPTER 2

LITERATURE REVIEW

INTRODUCTION

Carrier Signal – is a transmitted electromagnetic pulse or wave at a steady base frequency of alternation on which the information can be imposed by increasing signal strength, varying the base frequency, varying wave phase, or other means.

A Carrier System – is a circuit used to estimate and compensate for frequency and phase difference between a received signal's carrier wave and the receiver's oscillator for the purpose of coherent demodulation. In the transmitter of a communication carrier system, a carrier wave is modulated by a baseband signal. At the receiver the baseband information is extracted from the incoming modulated waveform.

REASONS FOR CARRIER EXTRACTION

- To improve both the transmitter's and receiver's efficiency.
- For proper coherent demodulation at the receiver.
- To save on the power that might be used to transmit carrier wave.

METHODS OF CARRIER RECOVERY

a) Multiplication Loop (squaring loop)- makes use of Mth order non-linear square law function preceded by a band pass filter to remove the modulation. Squaring of signal is a necessary operation which destroy the modulation and produce a frequency at f_c (f_c =cut off frequency), however, the squaring leads to enhancement of noise that increases the noise power level and results in an increase in the variance of the phase error[2].

b) Costas Loop- an estimate of a carrier phase is obtained by multiplying the input suppressed carrier plus noise with the output of the voltage control oscillator (VCO) and a 90° shifted version of the VCO signal, respectively, filtering the result of two multiplications and using filtered signal to control VCO phase and frequency[2].

c) Re-modulator Loop- incoming signal is demodulated and the message waveform is recovered. This baseband waveform is used to re-modulate the incoming signal. If the waveforms are rectangular and time aligned, the re-modulation procedure removes the modulation completely[2].

Other types of carrier recovery are just modification of the three types mentioned above.

LIMITATIONS OF COSTAS AND REMODULATOR LOOPS

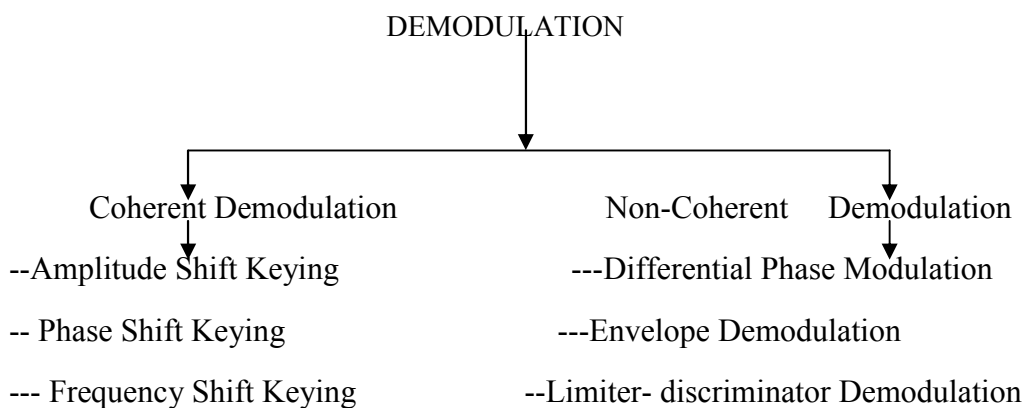
- ❖ Costas loop suffers from phase distortion of 180° i.e the recovered carrier may be either in phase or antiphase with the transmitted (suppressed) carrier. Amplitude of the signal is rectified on both the two arms which is corrupted by noise.
- ❖ Re-modulator loop can only receive only one data rate due to the requirement of the time alignment between the incoming modulated signal and the demodulated baseband signal before the multiplication of these two signals to remove the modulation. The delay introduced by the delay line used to obtain this time alignment must be changed appropriately each time a different data rate, other than the one for which the delay is set is to be received.

ADVANTAGES OF REMODULATOR LOOP

- It is not severely affected by noise as in Costas loop since rectification of signal amplitude takes place only in one arm.
- Due to time alignment, carrier recovery at the receiver is more efficient i.e. with little error in phase and frequency.

Coherent demodulation is when the receiver exploits knowledge of the carrier phase to detect the signals while Non-coherent demodulation assumes that the receiver has no knowledge of the carrier phase. Demodulation emphasizes on waveform recovery, and detection entails the process of signal decision[3].

Carrier recovery circuits are used in coherent demodulation.



PHASE SHIFT KEYING [PSK]

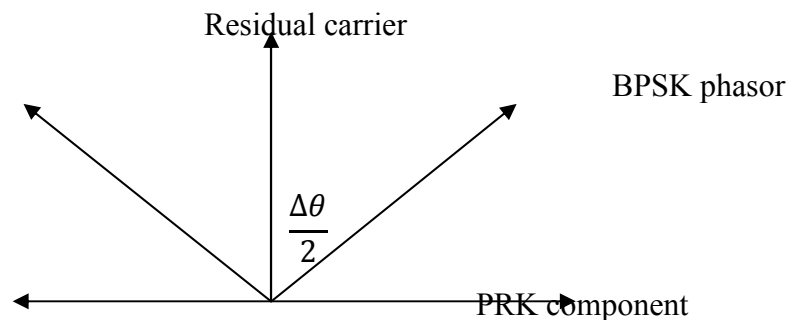
Involve the shifting of a carrier's phase among several discrete values. PSK of the carrier results when all binary digits from the information sequence are mapped into discrete phases of the carrier.

a) Binary Phase Shift Keying [BPSK]

It impresses baseband information onto a carrier by changing the carrier's phase in sympathy with the baseband digital data i.e

$$F(t) = \begin{cases} A\pi\left(\frac{t}{T}\right)\cos 2\pi f_c t & \text{for a digit 1} \\ A\pi\left(\frac{t}{T}\right)\cos(2\pi f_c t + \theta) & \text{for a digit 0} \end{cases}$$

For more general BPSK modulation where the difference between phasor states is less than 180° , the performance is most easily derived by resolving the allowed phasor states into a residual carrier and a reduced amplitude phase reversal keying (PRK) signal. The residual carrier, which contributes nothing to symbol detection, can be employed as a pilot transmission and used for carrier recovery purposes at the receiver. If the difference between phasor states is $\Delta\theta$ and BPSK modulator index m is defined by $m = \sin\left(\frac{\Delta\theta}{2}\right)$ Then m is the proportion of the transmitted signal voltage which conveys information and the corresponding proportion of total symbol energy is $m^2 = \sin^2\left(\frac{\Delta\theta}{2}\right) = \frac{1}{2}[1 - \cos\Delta\theta]$



$\cos\Delta\theta$ is the scalar products of the two symbol phasors. Denoting this quantity by the normalized correction coefficient δ then $m = \sqrt{\frac{1}{2}(1 - \delta)}$

The BPSK probability of symbol error is found by replacing E in

$$P_e = \frac{1}{2} [1 - \operatorname{erf}(\frac{E}{N})^{0.5}] \text{ by } m^2 E$$

$$P_e = \frac{1}{2} \left[1 - \operatorname{erf}m \left(\frac{E}{N} \right)^{0.5} \right] \text{ then}$$

$$P_e = \frac{1}{2} [1 - \operatorname{erf} \sqrt{(1 - \delta)}/\sqrt{2} (E/N)^{0.5}]$$

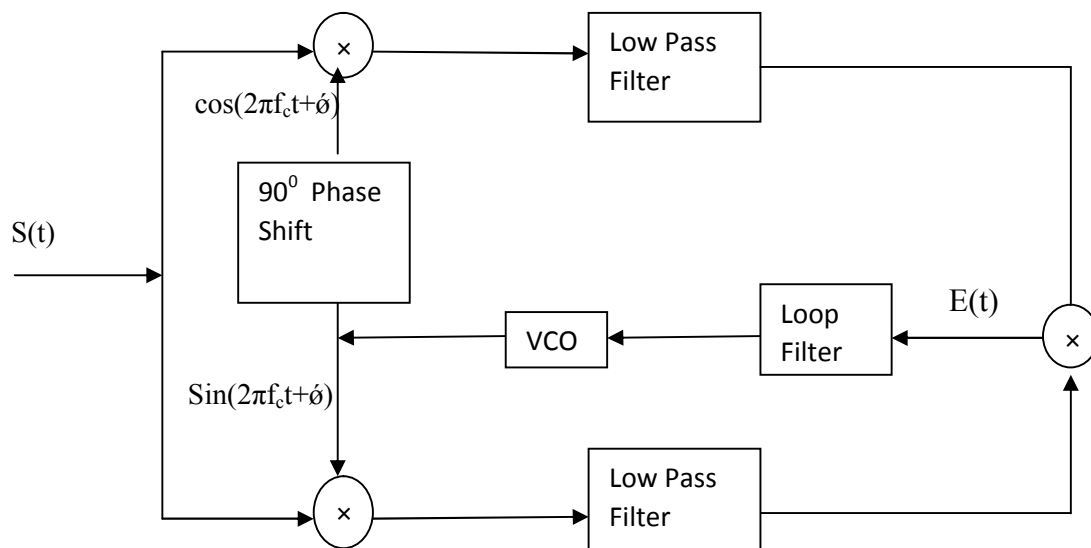
BPSK signals with phasor states separated by less than 180° contains discrete spectral lines at the carrier frequency and can therefore be demodulated without extraction of carrier. PRK signals however contain no such lines and carrier recovery must therefore be achieved using alternative methods[3].

b) Quaternary Phase Shift Keying (QPSK)

Four states are used, the adjacent ones being separated by 90° . Each phase is made to represent a pair of bits of a symbol i.e. 00, 01, 10, 11. Thus a pair of bits is sent each time the transmitter is keyed. Its performance in the presence of thermal noise, thus is the same as that of BPSK with respect to E/N . In the presence of such impairment as continuous wave interference and linear delay distortion, however bit error rate equation no longer hold and QPSK is found to degrade more rapidly than does BPSK.

CARRIER RECOVERY BY COSTAS LOOP

a) General Costas Loop



Costas loop is a method for generating a properly phased carrier for double-sideband suppressed carrier signal. The received signal is multiplied by $\cos(2\pi f_c t + \theta)$ and $\sin(2\pi f_c t + \theta)$ which are outputs from voltage control oscillator (vco). The two products are

$$Y_c(t) = [s(t) + n(t)] \cos(2\pi f_c t + \theta)$$

$$= \frac{1}{2} [A(t) + n_c(t)] \cos \Delta \theta + \frac{1}{2} n_s(t) \sin \Delta \theta + \text{double frequency term}$$

$$Y_c(t) = [s(t) + n(t)] \sin(2\pi f_c t + \theta)$$

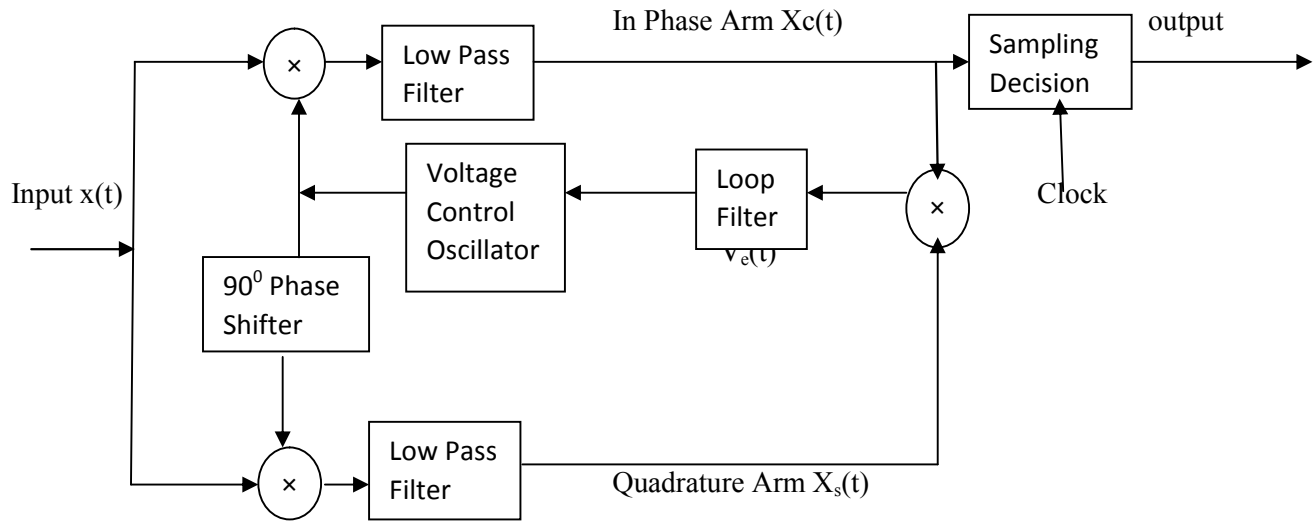
$$= \frac{1}{2} [A(t) + n_c(t)] \sin \Delta \theta - \frac{1}{2} n_s(t) \cos \Delta \theta + \text{double frequency term}$$

Where the phase error $\Delta \theta = \hat{\theta} - \theta$. The double frequency terms are eliminated by the low pass filter following the multiplication. An error signal is generated by multiplying the two outputs of the low pass filters Thus

$E(t) = \frac{1}{8} \{ [A(t) + n_c(t)]^2 - n_s^2(t) \} \sin(2\Delta \theta) - \frac{1}{4} n_s(t) [A(t) + n_c(t)] \cos(2\Delta \theta)$ This error signal is filtered by the loop filter whose output is the control voltage that drives the vco. Costas loop is

similar to phase locked loop. Note that the error signal into the loop filter consists of the desired term $A^2(t)\sin 2(\hat{\theta}-\theta)$ plus terms that involve signal \times noise and noise \times noise. Finally, the output of the vco contains a phase ambiguity of 180° necessitating the need for differential encoding of data prior to transmission and differential decoding at the demodulation[5].

b) BPSK Costas loop



Where $V_c(t)$ is the control voltage and $V_e(t)$ is the error voltage.

Carrier recovery circuit to be used depends closely on the chosen modulation. The received signal $x(t)$ is multiplied by the carrier recovered by the voltage controlled oscillator and by the same carrier with a 90° phase shift. The signals obtained are filtered in order to eliminate components with frequency close to twice the carrier frequency, and the resulting low pass signals $x_c(t)$ and $x_s(t)$ are multiplied together to give the error voltage $V_e(t)$. This is then filtered by the loop filter which determines the dynamic characteristics of the system. The control voltage obtained is applied to the voltage control oscillator in order to correct its phase. Sampling of the signal $x_c(t)$ or $x_s(t)$, depending on the synchronization point for the loop at the clock frequency, allows the demodulated signal to be obtained. The received signal represented as

$$x(t) = A(t)\cos(\omega_o t + \theta(t) + n(t)) \text{ with } \theta=0 \text{ or } \pi \text{ over interval of duration } T.$$

The voltage controlled oscillator provides the recovered carrier, with phase

$\hat{\theta}(t) = \theta_o(t) - \theta(t)$ for the phase error. The error voltage $v_e(t)$ can be expressed as

$$v_e(t) = \frac{1}{4} \left[(A(t) + n_c(t))^2 - n_s^2(t) \right] \sin 2\hat{\theta}(t) + \frac{1}{2} (A(t) + n_c(t)) n_s(t) \cos 2\hat{\theta}(t)$$

This error voltage is comparable to that obtained by squaring followed by a phase locked loop. In the absence of noise, with an unfiltered signal.

$$x(t) = A \cos(\omega_0 t + \theta(t)) \text{ and } v_e(t) = \frac{A^2}{4} \sin 2\theta(t)$$

BPSK can be modified by adding a limiter in the path of signal $x_c(t)$ which contains the transmitted information. The error voltage can then be expressed as

$v_e(t) = x_s(t) \text{sgn}(x_c(t))$ in the absence of noise with an unfiltered signal, we obtain

$$v_e(t) = \frac{A}{2} \sin \theta(t) \text{sgn}(\cos \theta(t))$$

Without a limiter $v_e(t) = x_c(t)x_s(t)$

With one limiter $v_e(t) = x_s(t) \text{sgn} x_c(t)$

With two limiters $v_e(t) = \text{sgn}(x_c(t) \text{sgn}(t))$ [5]

c) QPSK costas loop

The structure of the QPSK costas loop is similar to that of BPSK case. The difference is with the expression of error voltage which now becomes

$v_e(t) = x_c(t)x_s(t)(x_c^2(t) - x_s^2(t))$ Demodulation is carried out together with carrier recovery. Sampling of signals $x_c(t)$ and $x_s(t)$ provides the two demodulated sequences. The received signal is a QPSK modulated signal with noise. Let the received signal be given as

$$x(t) = A(t) \cos(\omega_0 t + \theta(t)) - B(t) \sin(\omega_0 t + \theta(t)) + n(t)$$

As the recovered carrier has phase $\theta_0(t)$, the phase error can be defined by $\phi(t) = \theta_0(t) - \theta(t)$ we then have

$$x_c(t) = \frac{1}{2} A(t) + n_c(t) \cos \phi(t) - \frac{1}{2} B(t) + n_s(t) \sin \phi(t)$$

$$x_s(t) = \frac{1}{2} A(t) + n_c(t) \sin \phi(t) + \frac{1}{2} B(t) + n_s(t) \cos \phi(t)$$

Calculating the error voltage leads to

$$\begin{aligned} v_e(t) = \frac{1}{16} \{ & \left[\frac{1}{4} \left[(A(t) + n_c(t))^2 - (B(t) + n_s(t))^2 \right]^2 - (A(t) + n_c(t))^2 (B(t) + n_s(t))^2 \right] \\ & \times \sin 4\phi(t) + \left[(A(t) + n_c(t))^2 - (B(t) + n_s(t))^2 \right] \\ & \times (A(t) + n_c(t)(B(t) + n_s(t) \cos 4\phi(t)) \} \end{aligned}$$

QPSK modulation is represented by shifts of 90° in the phase $\theta(t)$. The phase error is a function of $4\phi(t) = 4\theta_o(t) - 4\theta(t)$ and modulation has therefore been removed this expression. The coefficient of the term is $\cos 4\phi(t)$ is low. It can even be zero in the absence of noise. Minimization of the error voltage therefore requires minimization of the $\sin 4\phi(t)$ term. In the absence of noise with an unfiltered signal of amplitude A

$$v_e(t) = \frac{A^2}{64} \sin 4\phi$$

The characteristics of the equivalent phase detector is therefore $f(\phi) = \sin 4\phi$

If two limiters are used, the following operation can be carried out

$$v_e(t) = x_c(t) \operatorname{sgn} x_s(t) - x_s(t) \operatorname{sgn} x_c(t)$$

Without a limiter $v_e(t) = x_c(t)x_s(t)(x_c(t) - x_s(t))(x_c(t) + x_s(t))$ & $f(\phi) = \sin 4\phi$

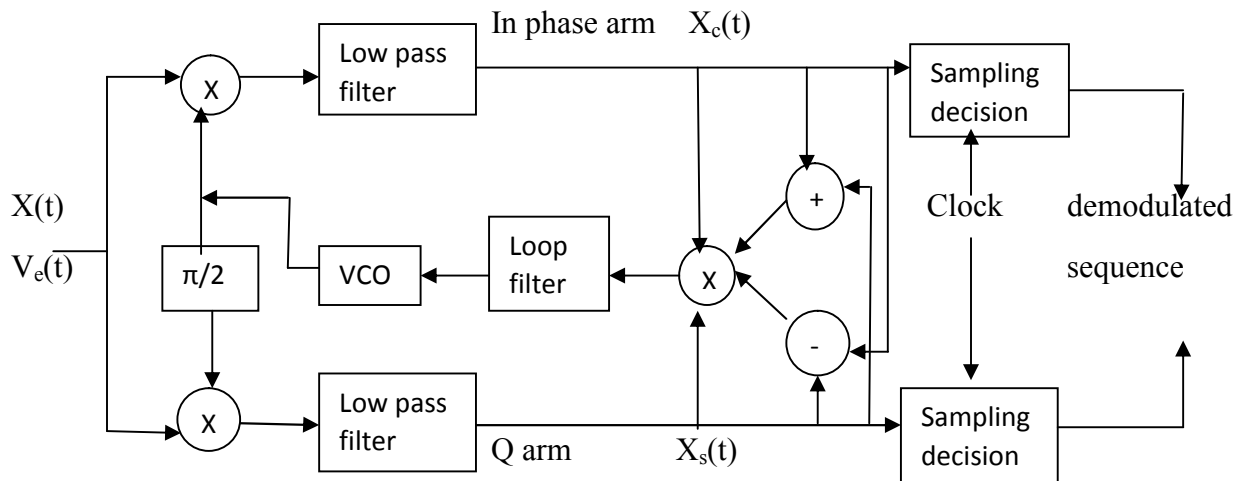
With one limiter $v_e(t) = x_c(t) \operatorname{sgn}(x_s(t)) - x_s(t) \operatorname{sgn}(x_c(t))$

And $f(\phi) = \cos \phi \operatorname{sgn}(\sin \phi)$ with two limiters the error voltage becomes

$$v_e(t) = \operatorname{sgn}(x_c(t)) \operatorname{sgn}(x_c(t) + x_s(t)) \operatorname{sgn}(x_c(t) - x_s(t))$$

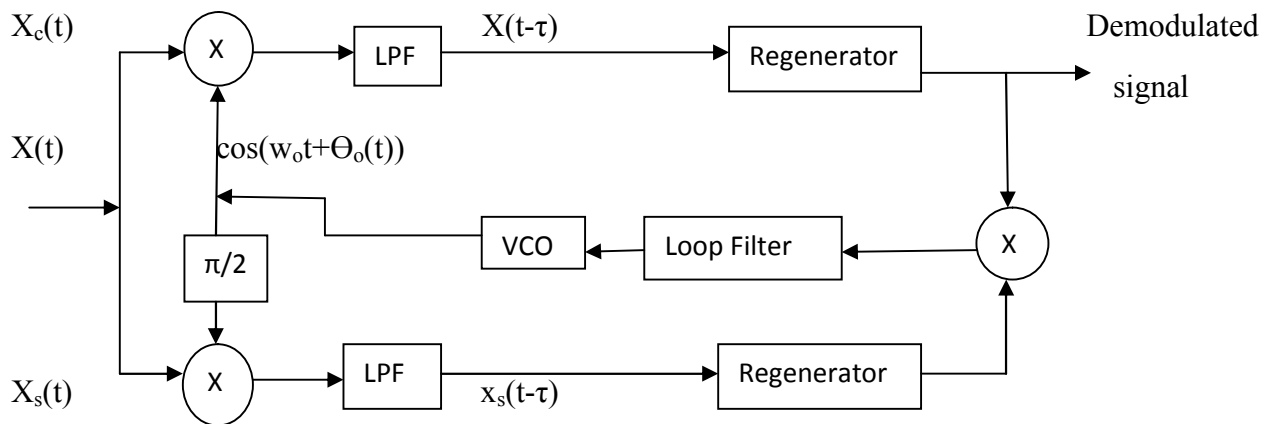
And $f(\phi) = \operatorname{sgn}(\sin 4\phi)$ The characteristics of the equivalent phase detector is given by

$f(\phi) = \cos \phi \operatorname{sgn}(\sin \phi) - \sin \phi \operatorname{sgn}(\cos \phi)$ limiters also make it possible to carry out the operation $v_e(t) = \operatorname{sgn}(x_c(t) \operatorname{sgn}(x_s(t)) + x_s(t) \operatorname{sgn}[x_c(t) - x_s(t)])$ The characteristics of the equivalent phase detector is $f(\phi) \operatorname{sgn}(\sin 4\phi)$



Other types of costas loop diagrams are shown on the next pages[5].

d) BPSK costas loop with a generator



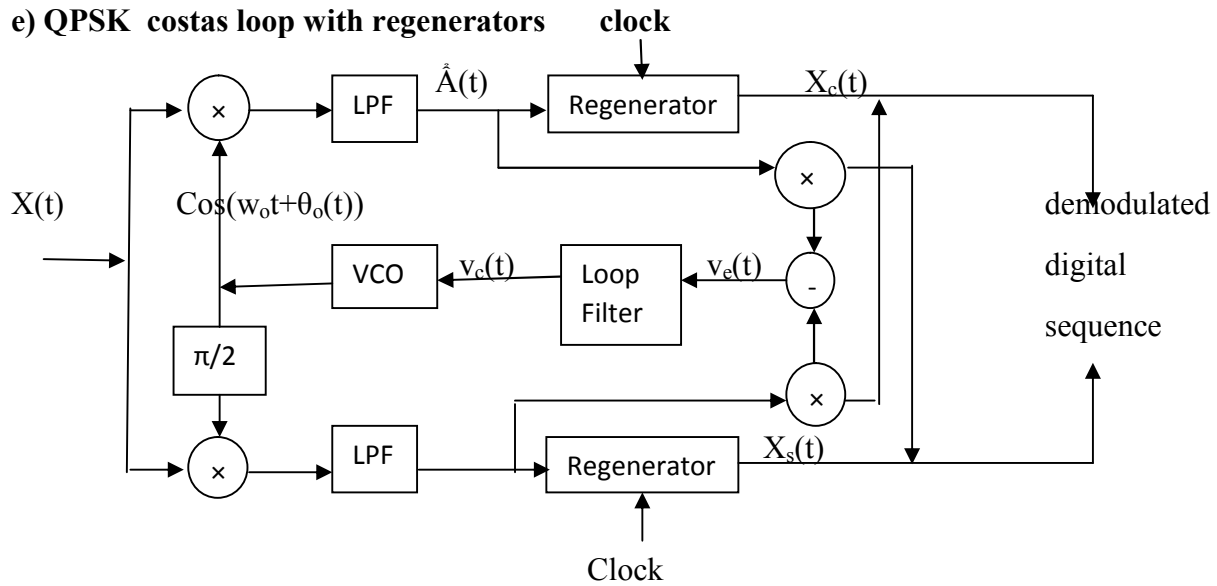
The regenerated signal $X(t)$ no longer contains noise but does on the other hand contain some errors. The error voltage for a given value ϕ of the phase error $\phi(t)$ is

$$v_e(t/\phi(t) = \phi) = (t)x_s(t) = \frac{1}{2}(t)[(A(t) + n_c(t))\sin\phi + n_s(t)\cos\phi(t)]$$

The statistical mean of the error voltage, calculated with error probabilities taken into account is[5]

$$E(v_e(t)) = \frac{1}{2}A^2(1 - 2p_e(\phi))\sin\phi$$

e) QPSK costas loop with regenerators



The error voltage is given by $v_e(t) = x_s(t)(t) - x_c(t)(t)$

This gives a mean of

$$E(A(t)(t)/\phi(t) = \phi) = E(B(t)(t)/\phi(t) = \phi) = A^2(1 - p_{e1}(\phi) - p_{e2}(\phi))$$

$$E(A(t)\square(t)/\phi(t)=\phi) = -E(B(t)\hat{A}(t)/\phi(t)=\phi) = A^2(p_{e1}(\phi) - p_{e2}(\phi))$$

Where

$$p_{e1}(\phi) = \frac{1}{2} \operatorname{erfc}(\sqrt{\frac{E}{N}}(\cos\phi - \sin\phi)) \text{ and } p_{e2}(\phi) = \frac{1}{2} \operatorname{erfc}(\sqrt{\frac{E}{N}}(\cos\phi + \sin\phi))$$

The error voltage condition on the phase error is

$$V_e(t)/\phi(t)=\phi = \frac{1}{2}[(A(t) + n_c(t))(t) + (B(t) + n_s(t)(t))\sin\phi - \frac{1}{2}[(A(t) + n_c(t)(t) - (B(t) + n_s(t)(t))\cos\phi$$

And its statistical mean is[5]

$$V_e(t)/\phi(t)=\phi = A^2[(1 - p_{e1}(\phi)) - p_{e2}(\phi)\sin\phi - (p_{e1}(\phi) - p_{e2}(\phi))\cos\phi$$

CARRIER RECOVERY BY REMODULATION

a) General introduction

The underlying principle of this method of carrier recovery is to eliminate the modulation of the received signal using the demodulated signal. The two possible approaches includes,

- a) Modulation, by the demodulated signal, of pure carrier produced by a voltage control oscillator and a comparison obtained in this way with the received signal. This received signal provides an error voltage allowing the oscillator frequency to be corrected. This is used in BPSK.
- b) Re-modulation of the received signal, by the demodulated signal. This operation removes modulation and provides an unmodulated carrier that can be filtered, either by filter or a phase locked loop. This is used in QPSK[5].

In this method, the incoming signal is demodulated and the message waveform is recovered. This baseband waveform is used to re-modulate the incoming signal, if the waveforms are rectangular and time aligned, the re-modulation procedure completely removes the modulation. The output of the balanced modulator has a pure carrier component at the input frequency and the phase-locked loop tracks the component. The re-modulator, however is typically implemented at low frequencies and cannot be used for multiple data rates due to time delays which impact the realization of the wideband synchronizer. Another re-modulator version imposes the recovered message modulation of the vcooutput so that both inputs to the phase detector are identically modulated. The low frequency product of the two such waveforms results in a DC component of the same amplitude as if the inputs had no modulation. This version can be applied to QPSK carrier recovery and data extraction. QPSK remodulator loop has been shown to exhibit a somewhat faster acquisition time when compared to a convention QPSK costasloop[5].

Re-modulation loop can receive only one data rate due to the requirement of the time alignment between the incoming modulated signal and the demodulated baseband signal before the multiplication of these two signals to remove modulation. The delay introduced by the delay time used to obtain this alignment must be changed appropriately each time a different data rate, other the one for which the delay is set, is to be received. Thus a re-modulation loop cannot be used in a multi-mission multiple data rate ground station.

Re-modulation loop is used in a range of frequencies below that of intermediate frequencies. An **intermediate frequency (IF)** is a frequency to which a carrier frequency is shifted as an intermediate step in transmission or reception. The intermediate frequency is created by mixing the carrier signal with a local oscillator signal resulting in a signal at the difference or beat frequency.

Reasons for using IF

At very high frequencies, signal processing circuitry performs poorly. Active devices such as

transistors cannot deliver much amplification. Ordinary circuits using capacitors and inductors must be replaced with cumbersome high frequency techniques such as striplines and waveguides. It is difficult to build amplifiers, filters, and detectors that can be tuned to different frequencies, but easy to build tunable oscillators. The main reason for using an intermediate frequency is to improve frequency selectivity.

Commonly used intermediate frequencies in FM range.(88MHz to 108MHz)

FM radio receivers: 262 kHz, 455 kHz, 1.6 MHz, 5.5 MHz, 10.7 MHz, 10.8 MHz, 11.2 MHz, 11.7 MHz, 11.8 MHz, 21.4 MHz, 75 MHz and 98 MHz. In double-conversion superheterodyne receivers, a first intermediate frequency of 10.7 MHz is often used, followed by a second intermediate frequency of 470 kHz. There are triple conversion designs used in police scanner receivers, high-end communications receivers, and many point-to-point microwave systems.

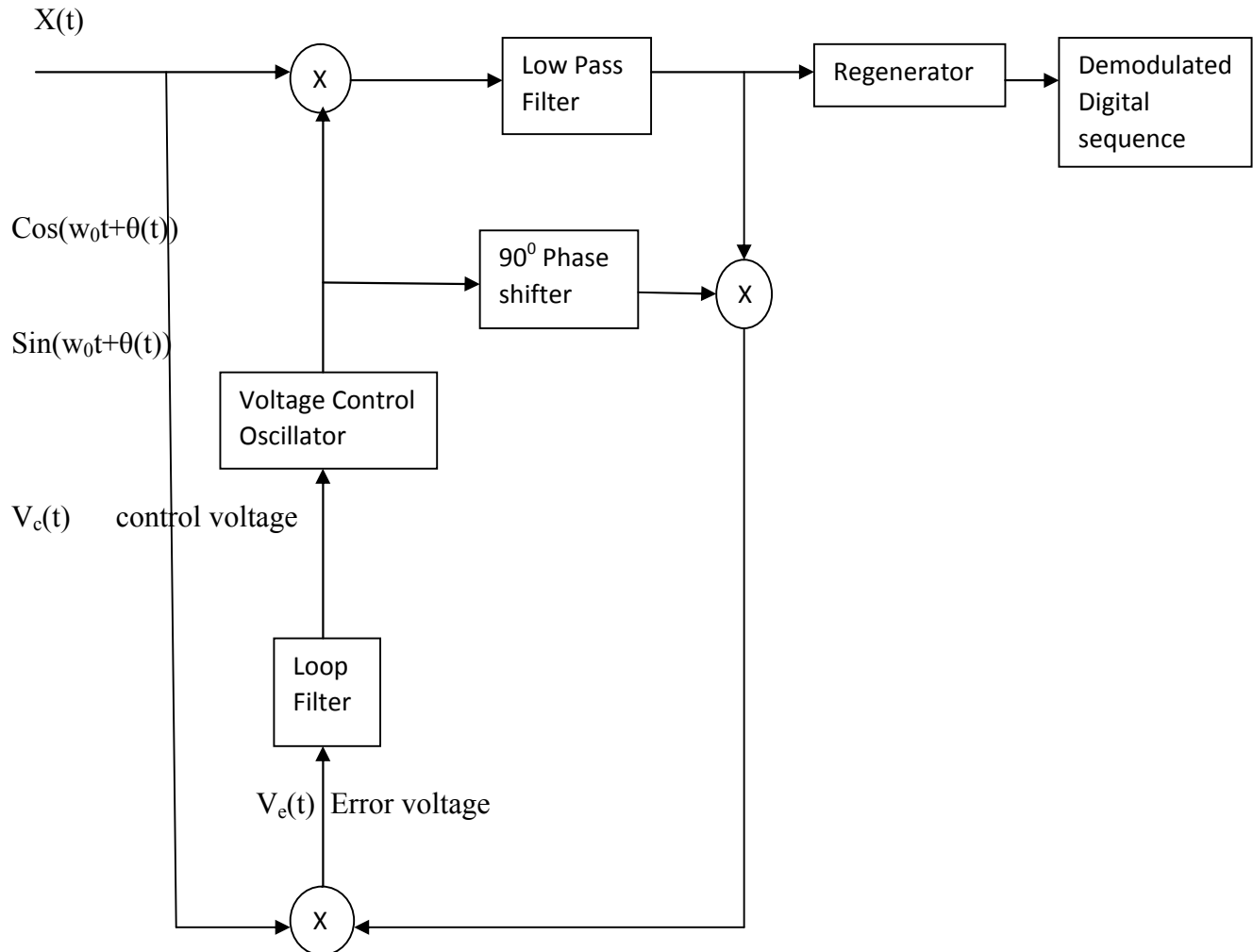
b) BPSK modulation The low pass component of the error voltage is given by

$$v_e(t) = \frac{1}{4} [A(t) + n_c(t)\cos\phi(t) - n_s(t)\sin\phi(t)] \times [A(t) + n_c(t)\sin\phi(t) + n_s(t)\cos\phi(t)]$$

$$= \frac{1}{8} [A(t) + n_c(t)]^2 - n_s^2(t) \sin 2\phi(t) + 2(A(t) + n_c(t))n_s(t)\cos 2\phi(t)]$$

The expression for this error voltage is comparable to that obtained for the carrier recovery by squaring followed by a phase locked loop or for the BPSK costas loop. In particular, there is once more a second order ambiguity on the phase of the carrier recovered. As with the case with the costas loop. A limiter or a regenerator, acting on $x_c(t)$, can be included in the circuit[5].

The circuit is shown on the next page.



BPSK re-modulator loop

c) QPSK modulation

The received signal is a QPSK modulated signal with noise

$$X(t) = A(t)\cos(\omega_c t + \theta(t)) - B(t)\sin(\omega_c t + \theta(t)) + n(t)$$

Multiplication of this signal by the recovered carrier and low pass filtering gives this

$$X_c(t) = \frac{1}{2} [A(t) + n_c(t)\cos\theta(t) - B(t) + n_s(t)\sin\theta(t)] \quad \text{and} \quad X_s(t) = \frac{1}{2} [A(t) + n_c(t)\sin\theta(t) + B(t) + n_s(t)\cos\theta(t)]$$

A phase shift of 90° in the received signal $X(t)$ leads to

$$X'(t) = (A(t) + n_c(t))\sin(\omega_c t + \theta(t)) - (B(t) + n_s(t))\cos(\omega_c t + \theta(t))$$

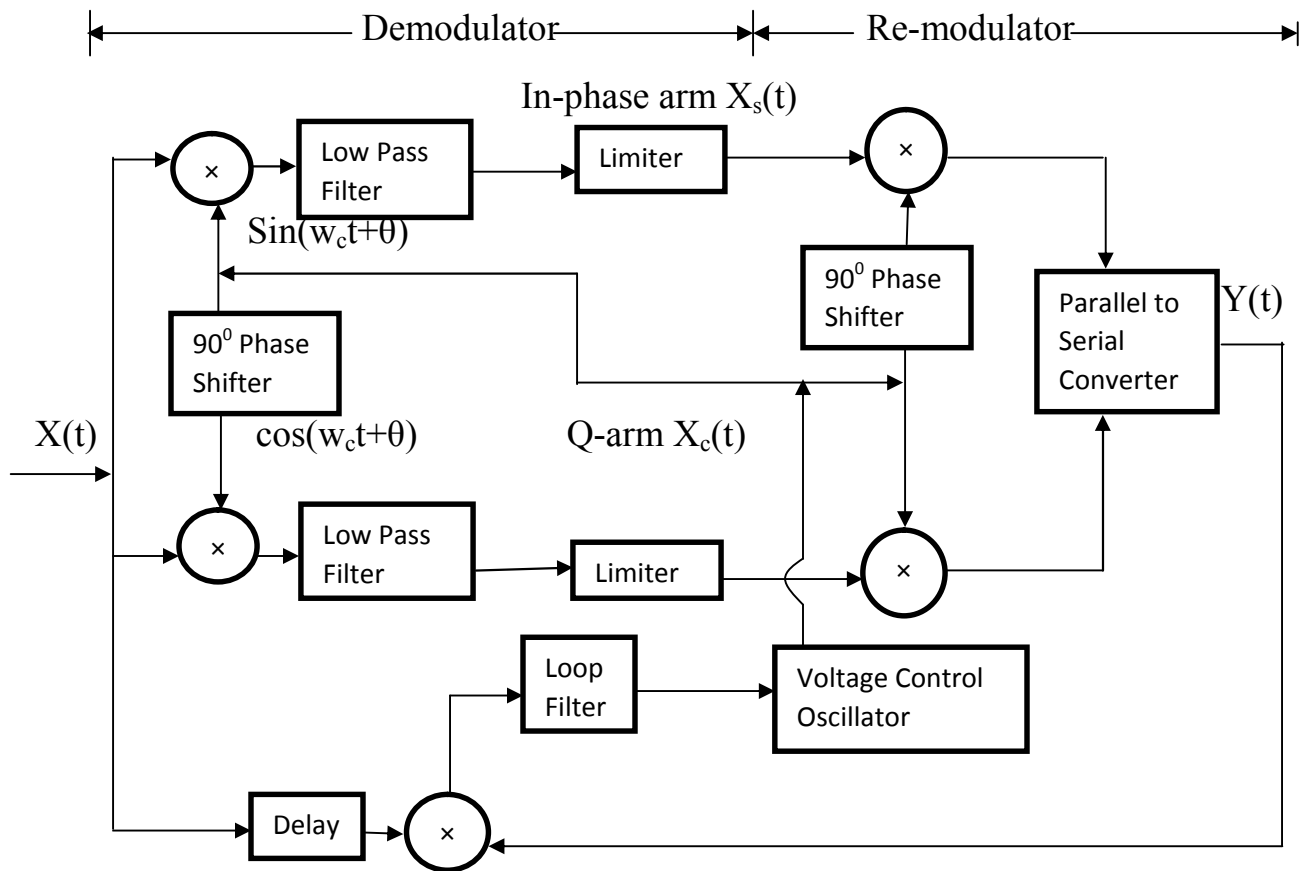
Re-modulation gives

$$Y_c(t) = x'(t)\text{sgn}(X_c(t)), \quad Y_s(t) = X(t)\text{sgn}(X_s(t))$$

The error voltage has the following low pass components

$$V_e(t) = (y_s(t) + y_c(t)) \cos(\omega_c t + \theta(t)) = X_c(t) \operatorname{sgn}(X_s(t)) - X_s(t) \operatorname{sgn}(X_c(t))$$

Multipliers multiplies the received signal and the carrier recovered. Low pass filter removes the double frequency term(harmonics) from the multiplier. Limiter ensures that peaks of noise above the signal peak is attenuated to avoid interference. Delay provides time alignment between received signal and demodulated baseband signal. Loop filter removes the harmonics from multiplier and its output used to control vco. Finally, parallel to serial converter convertes parallel data into serial output[5].



QPSK re-modulator loop

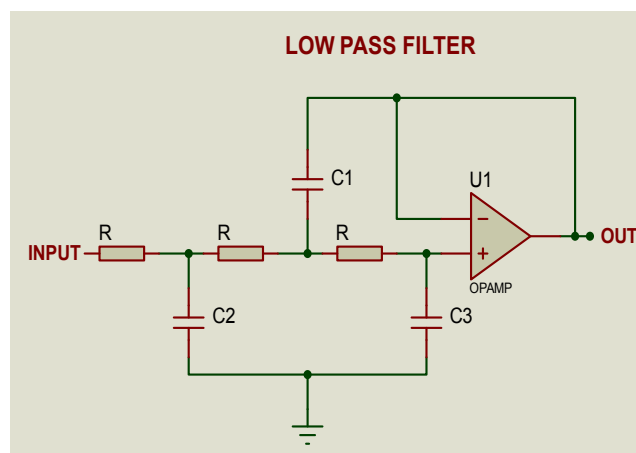
- 1) **Low Pass Filter** – It allows all the frequencies below 100MHz to pass unattenuated and attenuate frequencies above the cut-off frequency which is 100MHz. In the design, the filter eliminates the double frequency term from the multiplier. Loop filter also does the same activity.
- 2) **Multiplier** – It multiplies the carrier recovered and the incoming QPSK modulated(received) signal.

- 3) **Limiter** – It amplifies both the actual signal and noise. Voltage reference of the limiter is set to that of the input signal amplitude so that at any one point the noise amplitude does not exceed that of the signal.
- 4) **Delay** – Provides the time alignment between the incoming QPSK modulated signal and the demodulated signal.
- 5) **Phase shifter** – It shifts the phase of the carrier signal recovered by 90^0 . The shifted version of the carrier is used in the quadrature arm.
- 6) **Parallel to serial converter** which converts the data received from the in-phase arm and the quadrature arm into serial output.
- 7) **voltage control oscillator**—Is controlled by the output of the loop filter to provide a stable voltage over a certain range of frequencies {88MHz to 108MHz}. It also corrects the phase of the carrier signal recovered.

d) Description of the circuits making the QPSK re-modulator loop.

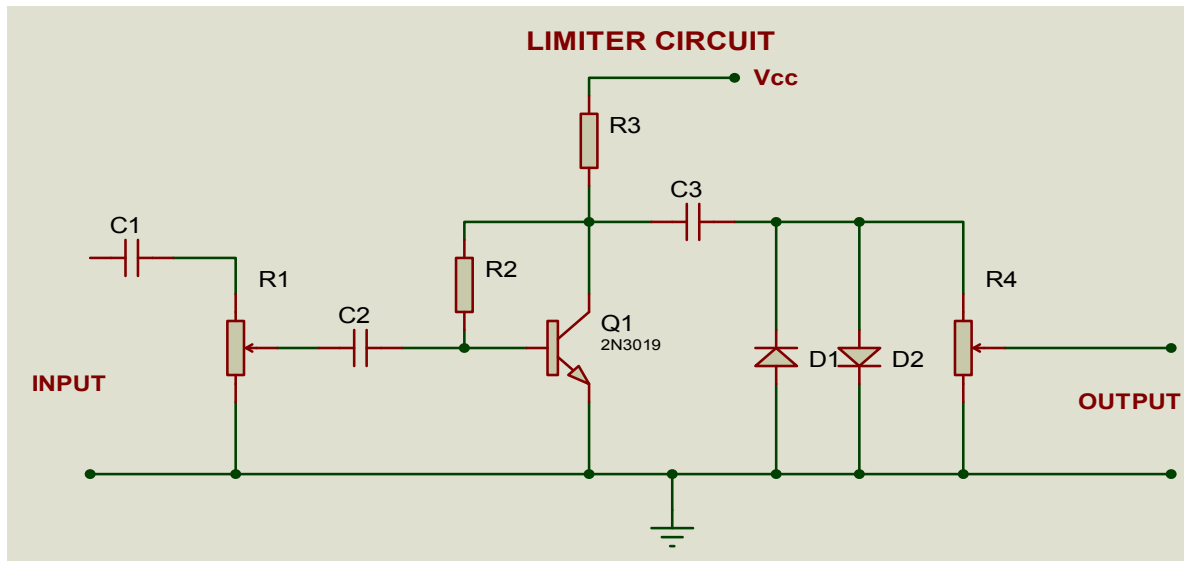
1. Low Pass Filter

Has the property that low frequency excitation signal components down to and including direct current, are transmitted, while high frequency components upto and including infinite ones are blocked. The range of low frequencies, which are passed, is called passband or the bandwidth of the filter and extends from $\omega=0$ to $\omega=\omega_c$ rads/seconds (f_c in Hz). The highest frequency to be transmitted is ω_c called cut off frequency. Frequencies above cutoff are prevented from passing through the filter and they constitute the filter stopband. The parameters to be considered includes; A_p ---dB attenuation in the passband, A_s --- dB attenuation in the stop band, f_p --- frequency at which A_p occurs, f_s ---frequency at which A_s occurs, sampling frequency which must be twice that of cutoff frequency, filter order[7].



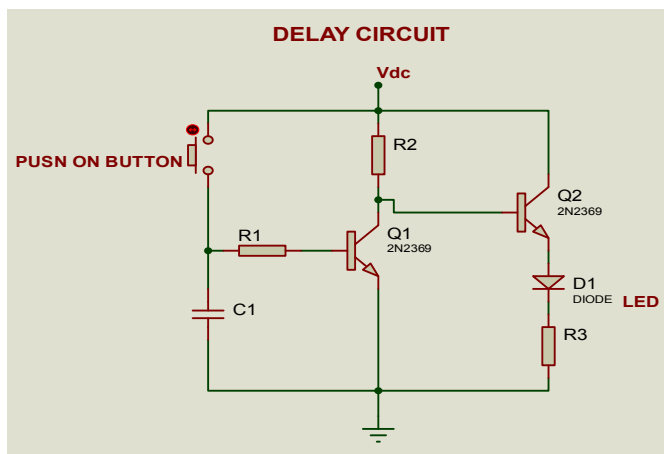
2. Limiters A limiter is a circuit that allows signals below a specified input power to pass unaffected while attenuating the peaks of stronger signals that exceed this input power. An ideal limiter constrains a signal to below (or above) a particular specified value, the break point. Both signal and noise are fed into the limiter and both of them are amplified equally, but diodes in the limiter automatically limit the peak to peak output swing. The noise peaks will not exceed signal output therefore the received signal will be far more intelligible. Diode based limiters are

instantaneous, simple in design and have a more accurate loudness response but suffers from distortion in the clipping region. The diodes voltage drop remains fairly constant throughout the operating range, and it is this property that is exploited in diode based limiter circuit. Limiter is actually a specialized form of audio compressors[9].



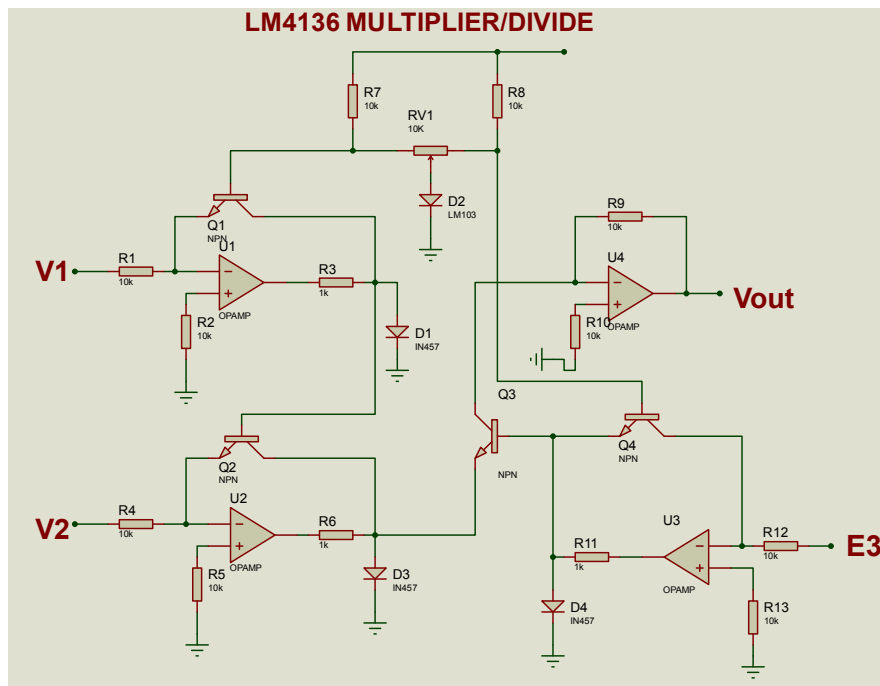
3. Delay Element

In most electronic circuits, a delay in time of some input signals is always important. This delay is always achieved by using a delay line circuit. The delay circuit provides time alignment between the QPSK modulated signal and the demodulated signal.



On pressing the ON button, the voltage from the supply enters the base of Q2 switching it ON thereby making the LED to light, the capacitor C1 is charged. When the supply is switched OFF, the charged capacitor discharges through Q1 making the LED to continue lighting for some time. Propagation delay time is the interval of time required after an input signal has been applied for the resulting output change to occur.

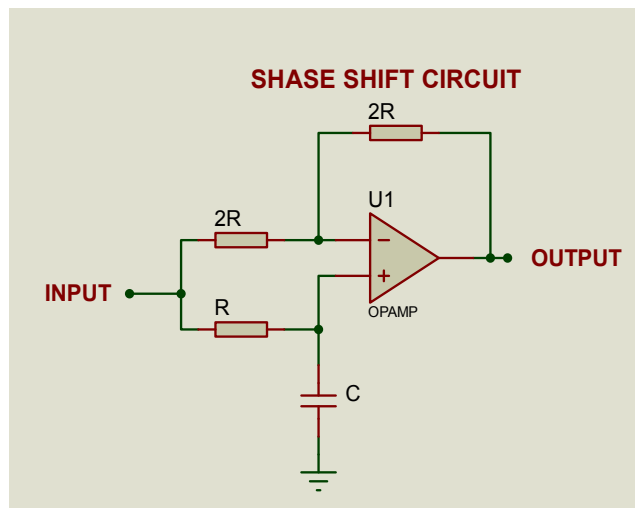
4. Multiplier



It multiplies the two signals which are the incoming QPSK modulated signal and the carrier recovered by the voltage controlled oscillator. The output voltage of this circuit at any value of time is proportional to the instantaneous product of two separate input signals. The DC bias requirements for multiplier chips are typically the same as those for most of OP-AMPS. A primary application of multiplier is to act as the balanced modulator used in communication systems and in carrier automatic control system to shift the frequency components of a signal to higher frequency range to ease the burden of signal transmission and processing.

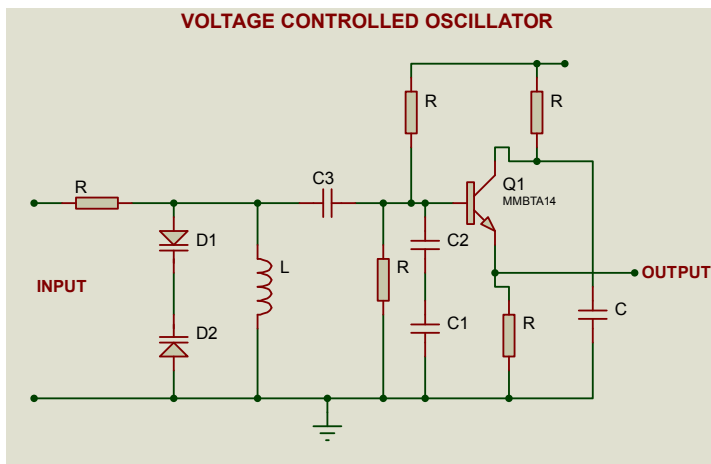
5. Phase Shift Circuit

A common operation required in electronic circuit design is the process of producing phase shift at a given frequency. All reactive networks are capable of producing phase shift, but majority of such circuits have amplitude response functions that vary with frequency which limits their usefulness in carefully controlled situations. The phase shift used here provides a 90° phase shift to the carrier signal recovered by the voltage controlled oscillator[8].



6. Voltage Controlled Oscillator

Is an electronic oscillator whose oscillation frequency is controlled by a voltage input. The applied input voltage determines the instantaneous oscillation frequency. Consequently modulating signals applied to the voltage controlled oscillator input may cause frequency modulation or phasemodulation. Bipolar junction transistors has a low input impedance and is current driven while field effect transistor has high input impedance and is voltage driven. The high input impedance of the FET is able to maintain the quality factor of the tuned circuit and this should give a better performance interms of phase noise performance where the quality factor of the tuned circuit is a key factor in the reduction of phase noise. Flicker noise generated by the devices is another factor to be considered since the oscillators are non-linear circuits and as a result the flicker noise is modulated onto the voltage controlled oscillator as sidebands and this manifest itself as phase noise. BJT offer a lower level of flicker noise. Tuning of VCO is achieved by making the variable capacitor from varacter diodes. The tune voltage for VCO can then be applied to the varacters[14].



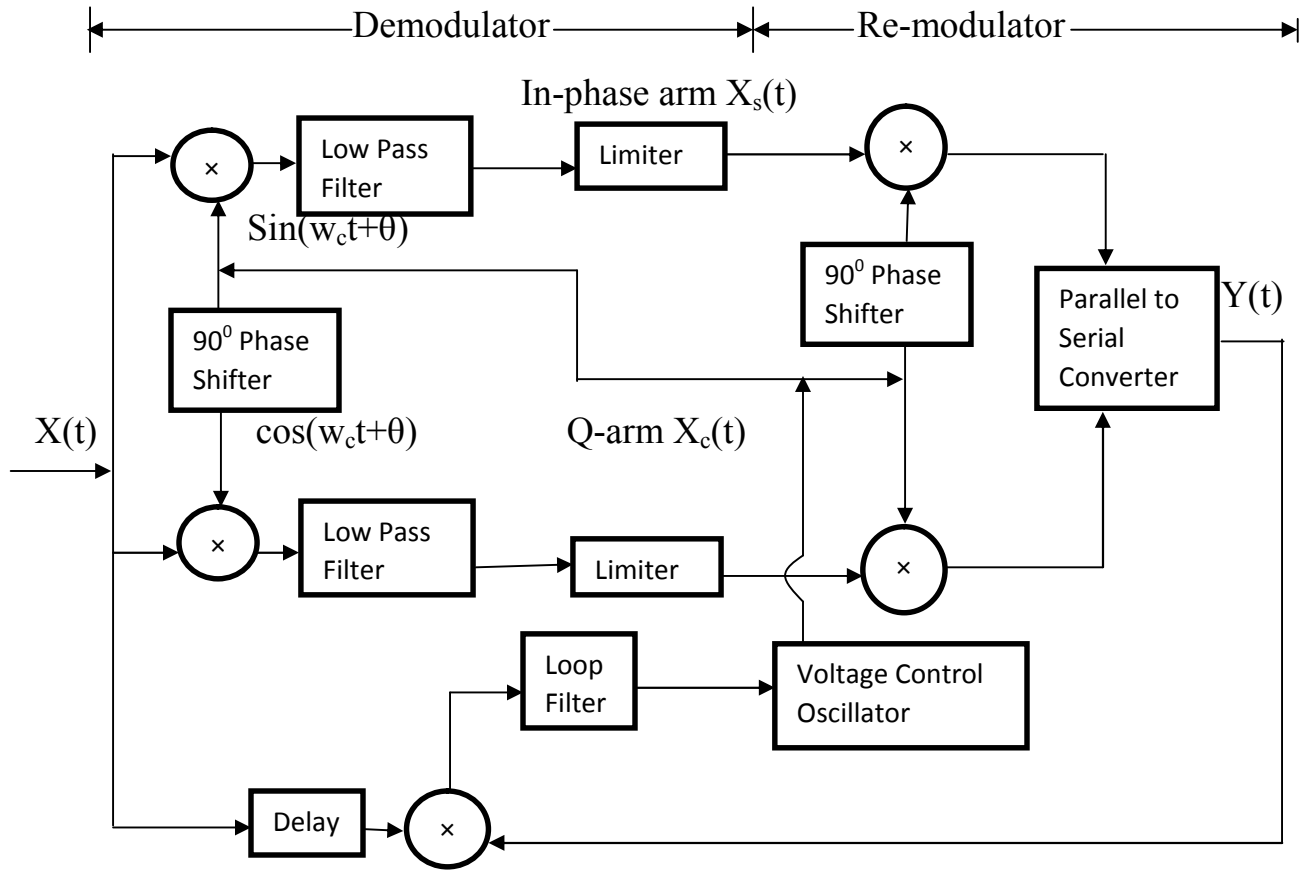
7. Parallel to serial converter

It store parallel data and gives out a serial output when a clock pulse is applied to it. For the project purpose a summer in the simulink is going to be used to add a signal at the quarature arm with that of the in phase arm and its output multiplied with the incoming signal to control the voltage control oscillator.

CHAPTER 3

DESIGN OF CARRIER RECOVERY BY REMODULATION IN QPSK

a) Design Block Diagram.



QPSK re-modulator loop

b) Principle of operation

In this method, the incoming signal is demodulated and the message waveform is recovered. This baseband waveform is used to re-modulate the incoming signal. If the waveforms are rectangular and time aligned, then the re-modulation procedure removes the modulation completely.

Demodulator- The output of voltage control oscillator (VCO) is passed through the 90° phase shifter. The input signal $X(t)$ is multiplied by the output of vco in the in-phase arm and the shifted version of vco output in the quadrature arm. Both the two multiplied signals are taken to low pass filter to remove the double frequency term or the harmonics from multiplier. Signal together with the noise is then taken to limiter which then amplify them. The limiter automatically limits the peak to peak output swing to the input voltage so that the noise amplitude does not exceed the actual signal amplitude. **Re-modulator-** The output of the limiter in I-arm is multiplied by the shifted output of the vco while the output of the limiter in the Q-arm

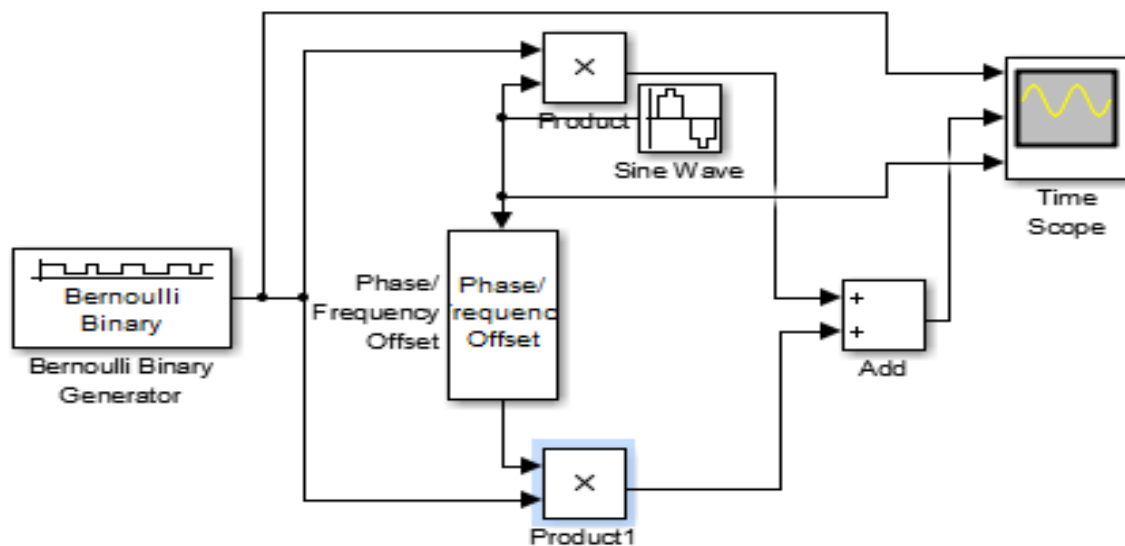
is multiplied by the output of vco. The two multiplied signals are taken to parallel to serial converter and its output multiplied with that of the delay and the resulting waveform taken to the loop filter which is just a low pass filter to remove harmonics from the multiplier. The output of the loop filter which is the carrier waveform is used to control the VCO.

c) Design of circuits that make the loop

The circuit consists of the following sub-circuits

- i. Low Pass Filter
- ii. Multipliers
- iii. Limiters
- iv. Delay Element
- v. Parallel to Serial Converter
- vi. Voltage Control Oscillator
- vii. 90° phase Shifter

QPSK modulation.



The parameters were set as follows; Bernoulli binary generator:- probability of a zero is 0.5, initial speed is 61 and sampling time is 0.01. sine wave:- frequency can be varied and phase is 1.5708rads corresponding to 90 degrees.

Low Pass Filter Sampling frequency is 500MHz, Bandstop frequency is 108MHz, bandpass frequency is 100MHz, passband ripple is 6dB, stopband attenuation is 60dB. The filter order was calculated as follows;

$$n = \frac{\log \frac{\epsilon_2}{\epsilon_1}}{\log \frac{f_p}{f_s}}$$

Where $\epsilon_1 = \sqrt{(10^{(0.1 \times A_p)} - 1)} = 1.7266$ A_p (passband ripple)=6dB

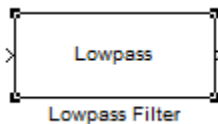
$\epsilon_2 = \sqrt{(10^{(0.1 \times A_s)} - 1)} = 999.9995$ A_s (stopband attenuation)=60dB

$$\log \frac{\epsilon_2}{\epsilon_1} = 2.7628$$

$$\log \frac{f_p}{f_s} = \frac{108}{100} = 0.0334$$

$$\text{filter order, } n = \frac{2.7628}{0.0334} = 82.718 \approx 83$$

f_s is the stopband frequency and f_p is the passband frequency. Three FIR filters are used, two in the quadrature and inphase arm and one before the VCO. The FIR digital filter was designed in matlab Simulink by feeding the calculated parameters in the filter's dialog box.



Low pass filter block

Multiplier

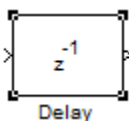
Five of them will be required in the project implementation in Simulink. Its settings are as follows; multiplication is elementwise, inputs are two and sample time is -1 for inherited.



Mutiplier Simulink block

Delay Element

The delay element delays the input signal for a specified time. Here a discrete unit delay is used. The delay element can be varied to provide better time alignment between the QPSK modulation signal and demodulated signal. Its settings were as follows; delay length is 2, initial condition is 0, external reset rising edge, input processing is elements as channels(sampled based) and sample time is -1 for inherited.



Delay block in simulink

Limiters/saturation

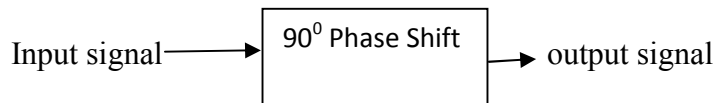
Used to limit the signal to a specified input amplitude so that the noise peak does not exceed the actual signal amplitude. Its settings are as follows; upper limit is 4, lower limit is -4 and sample time is -1 for inherited.



Limiters/saturation Simulink block

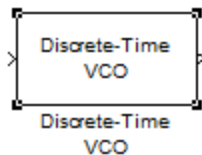
Phase Shift circuit

This circuit shifts the phase of the incoming signal by 90° . Its settings are as follows; phase offset(deg) is 90° , frequency offset from port is not enabled and frequency offset is 0.



Discrete Time Voltage Controlled oscillator (VCO)

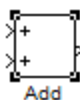
It corrects the phase of the carrier signal. Its settings are as follows; input amplitude is 2, quiescent frequency (Hz) is varied in accordance with the carrier frequency, input sensitivity (Hz/V) is 0.5, initial phase (rad) is 0 and sample time (s) is 0.01



VCO Simulink block

Summer

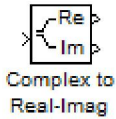
Used to combine the inphase signal and the quadrature signal. Its settings are as follows; icon shape is round, list of signs is ++ and sample time is -1 for inherited.



Simulink summer block

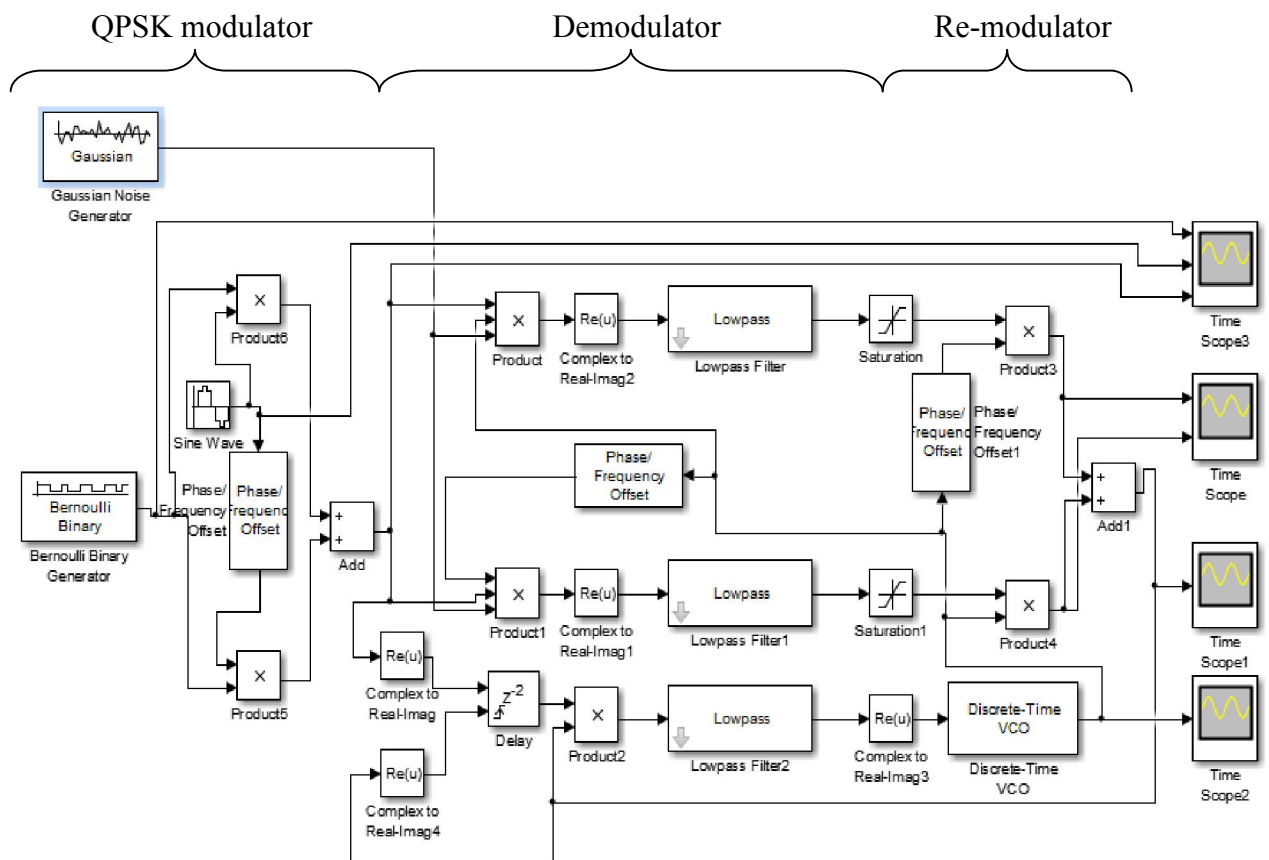
Complex to real and imaginary

It ensure that only real signals drive the blocks used in the design.



Complex to real-imaginary Simulink block

d)Implementation of carrier recovery by re-modulation in QPSK in simulink



Time scope is for measuring the signal from the inphase and quadrature arms. Time scope 1 is for measuring the resulting signal got after combining the inphase and quadrature signals. Time scope 2 is for measuring the carrier recovered signal (output of VCO). Time scope 3 is for measuring the signals in the simple QPSK modulator circuit.

e) Summary table for the block parameters used in the circuit

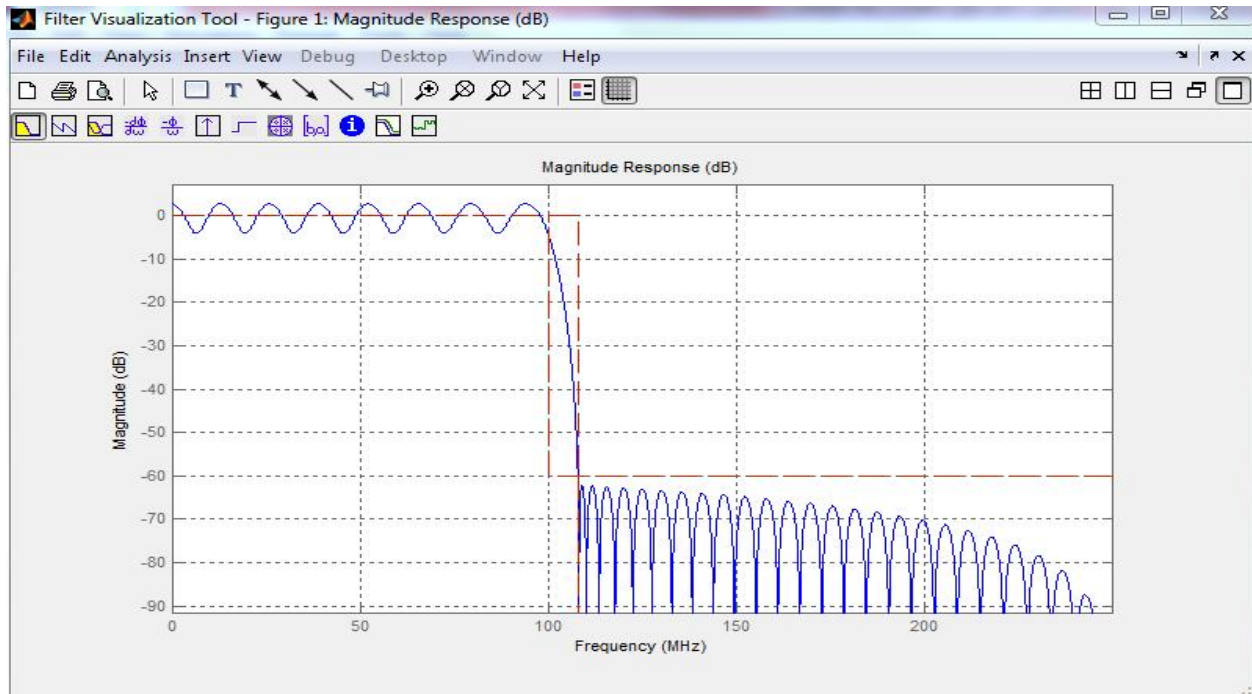
NAME OF THE BLOCK	BLOCK PARAMETER	PARAMETER SPECIFICATION
1. Bernoulli generator	probability of a zero	0.5
	initial speed	61
	sampling time	0.01
2. sine generator	frequency	Varied from 3rad/sec to 10rad/s
	phase	1.5708 rads
3. Low Pass Filter	Sampling frequency	500MHz
	Stop band edge frequency	108MHz
	Pass band edge frequency	100MHz
	Stop band attenuation	60dB
	Pass band ripple	6dB
	Filter order	83
	Filter type	FIR
4. limiter/saturation	Design method	Equiripple
	Upper limit	4
	Lower limit	-4
	Sample time	-1 for inherited
5. Discrete Time VCO	Output amplitude	2
	Quiescent frequency (Hz)	Set according to carrier frequency
	Input sensitivity (Hz/v)	0.5
	Initial Phase (rad)	0
	Sample time	0.01
6. Phase shift Circuit	Phase offset (deg)	90
	Frequency offset from port	Not enabled
	Frequency offset (Hz)	0
7. Multiplier/product	Number of inputs	2
	Sample time	-1 for inherited
	Multiplication	Elementwise
8. Delay element	Delay length	2
	Initial condition	0
	External reset	Rising edge
	Input processing	Elements as channels
9. Summer	Sample time	-1 for inherited
	Icon shape	round
	List of signs	++
10. Complex to real and imaginary	Sample time	-1 for inherited
	Output	Real
	Sample time	1

CHAPTER 4

RESULTS, DISCUSSIONS AND ANALYSIS

a) Results

Low Pass Filter response



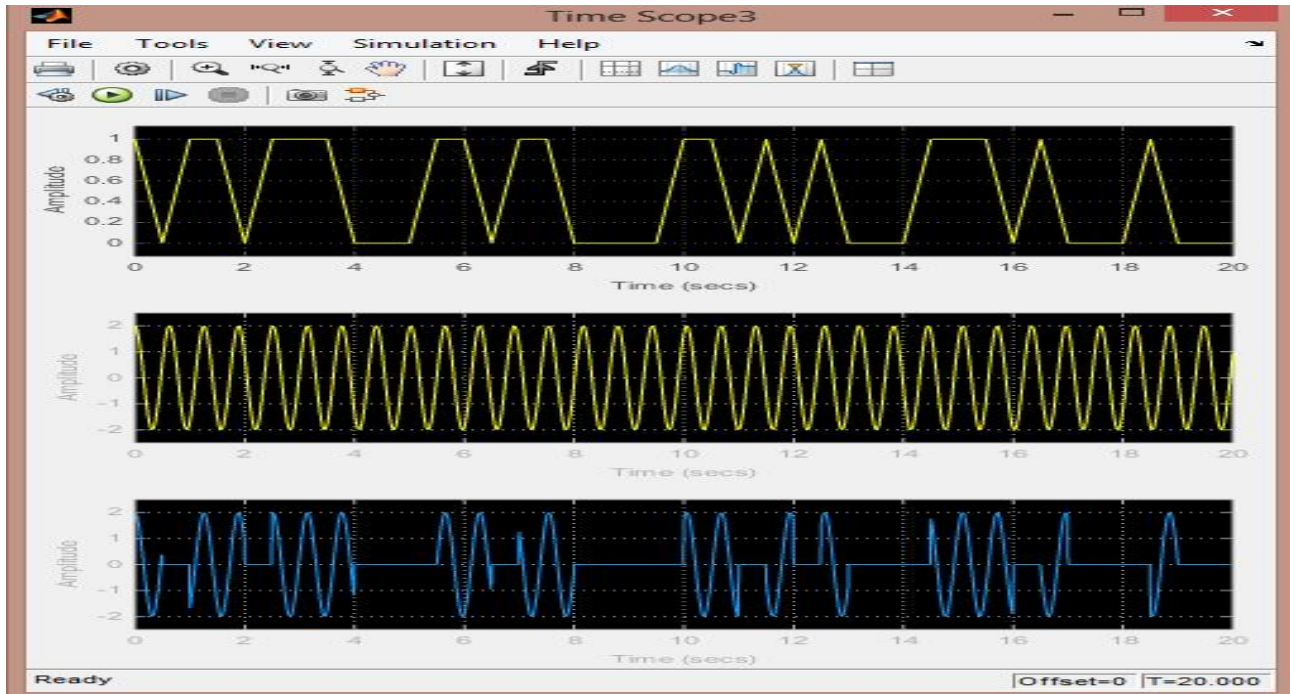
1. Carrier signal of 10 rads/sec

QPSK modulator signals

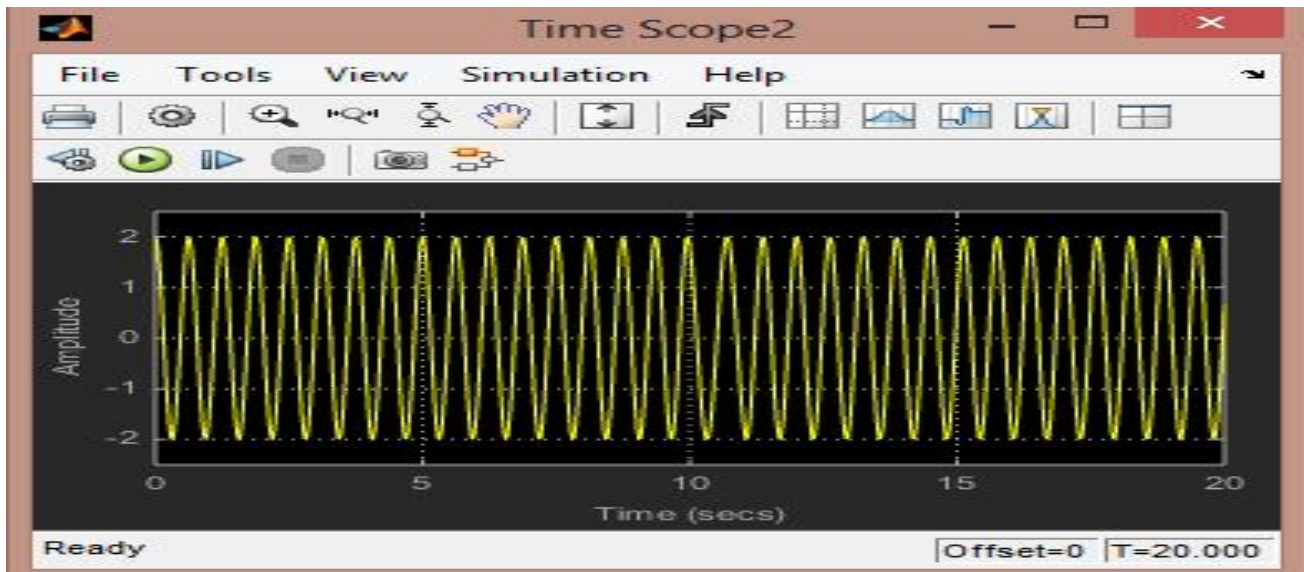
Top signal represents the message signal

Middle signal represents carrier signal used in QPSK modulation

Bottom signal represents QPSK modulated signal



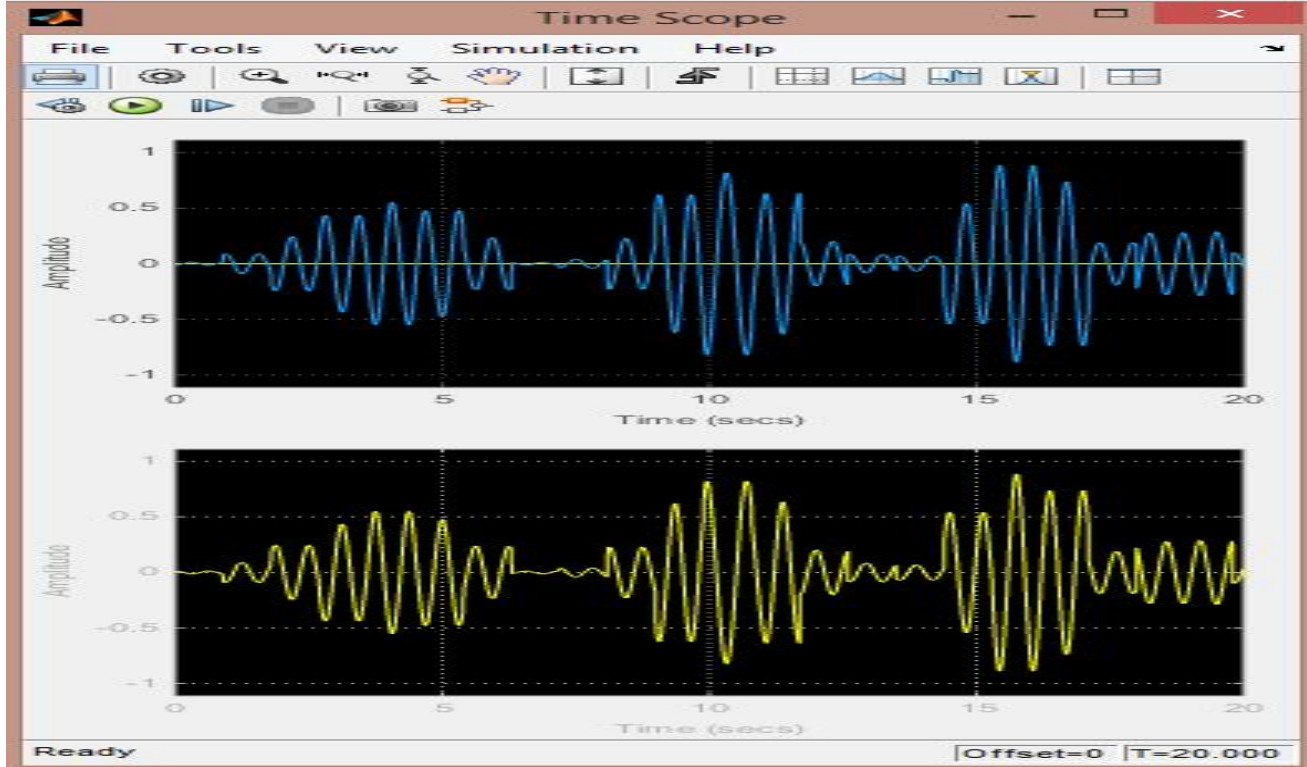
Carrier signal recovered at 10 rads/sec



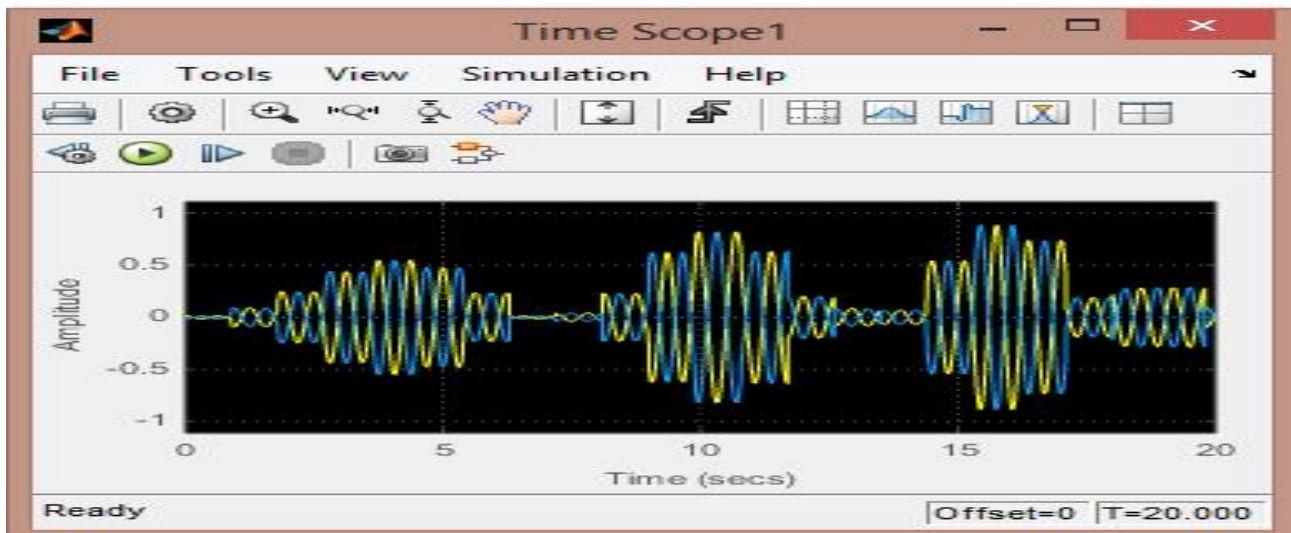
Inphase and Quadrature arm signal from the re-modulator side

Top signal represents that from inphase arm

Bottom signal represents that from quadrature arm



Combination of Inphase and Quadrature signals



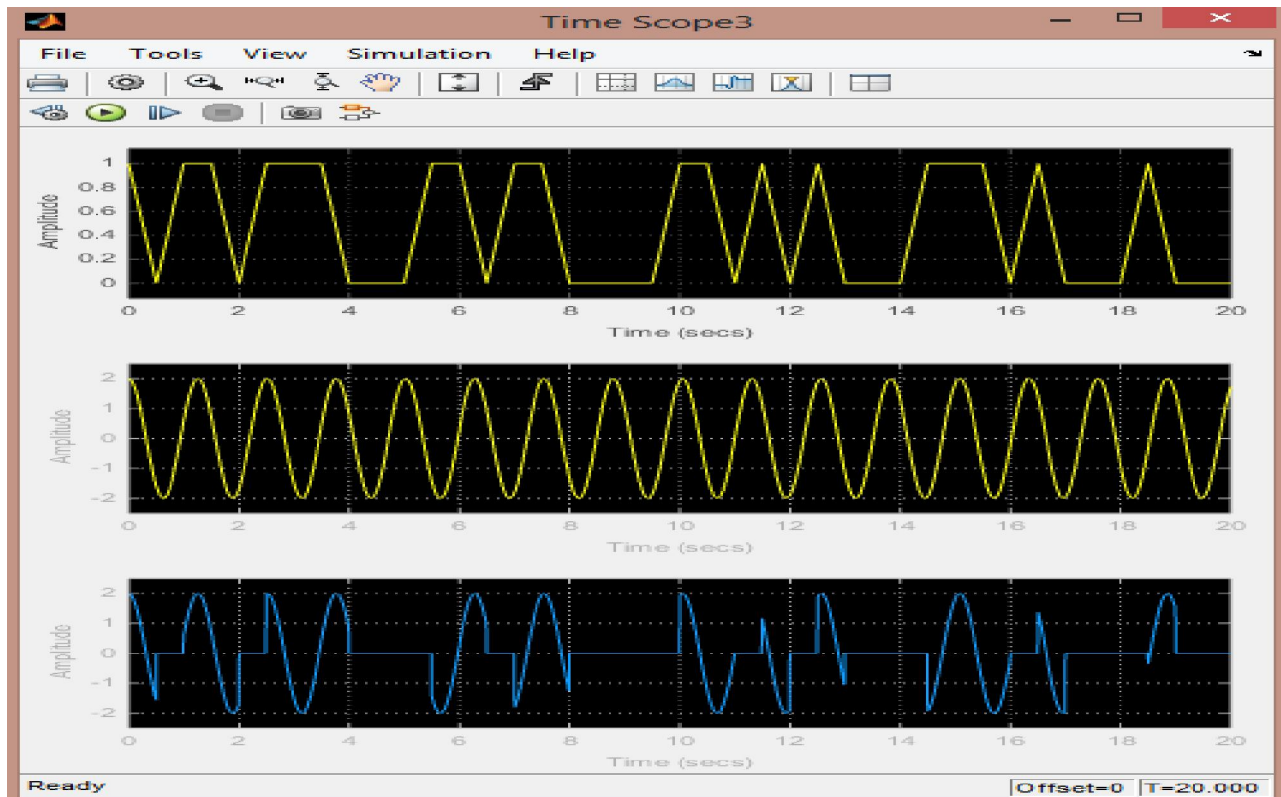
2. Carrier signal of 5 rads/sec

QPSK modulator signals

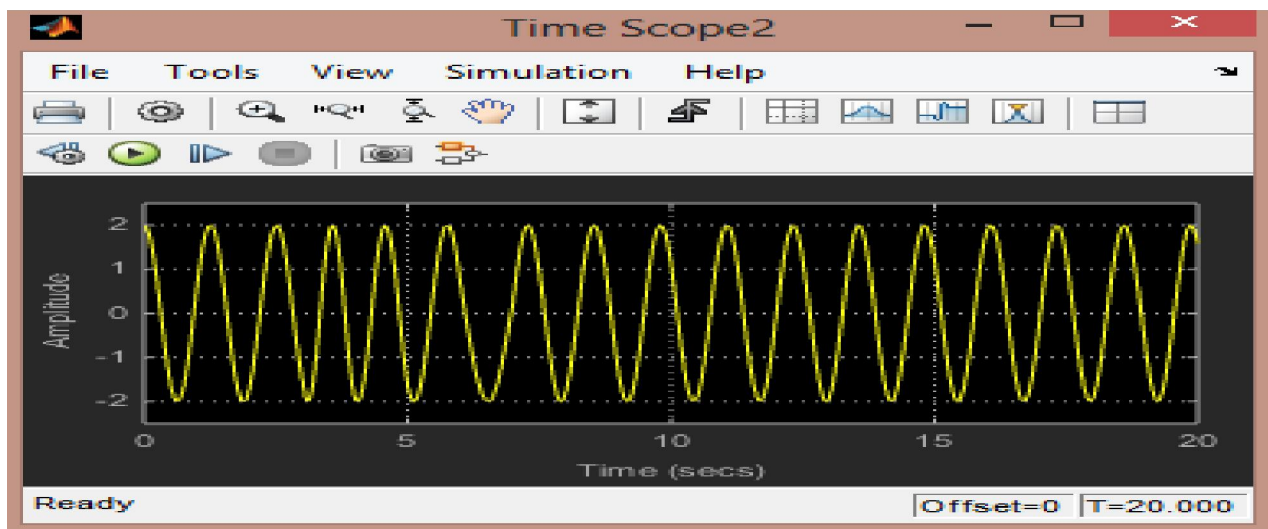
Top signal represents the message signal

Middle signal represents carrier signal used in QPSK modulation

Bottom signal represents QPSK modulated signal



Carrier signal recovered at 5 rads/sec



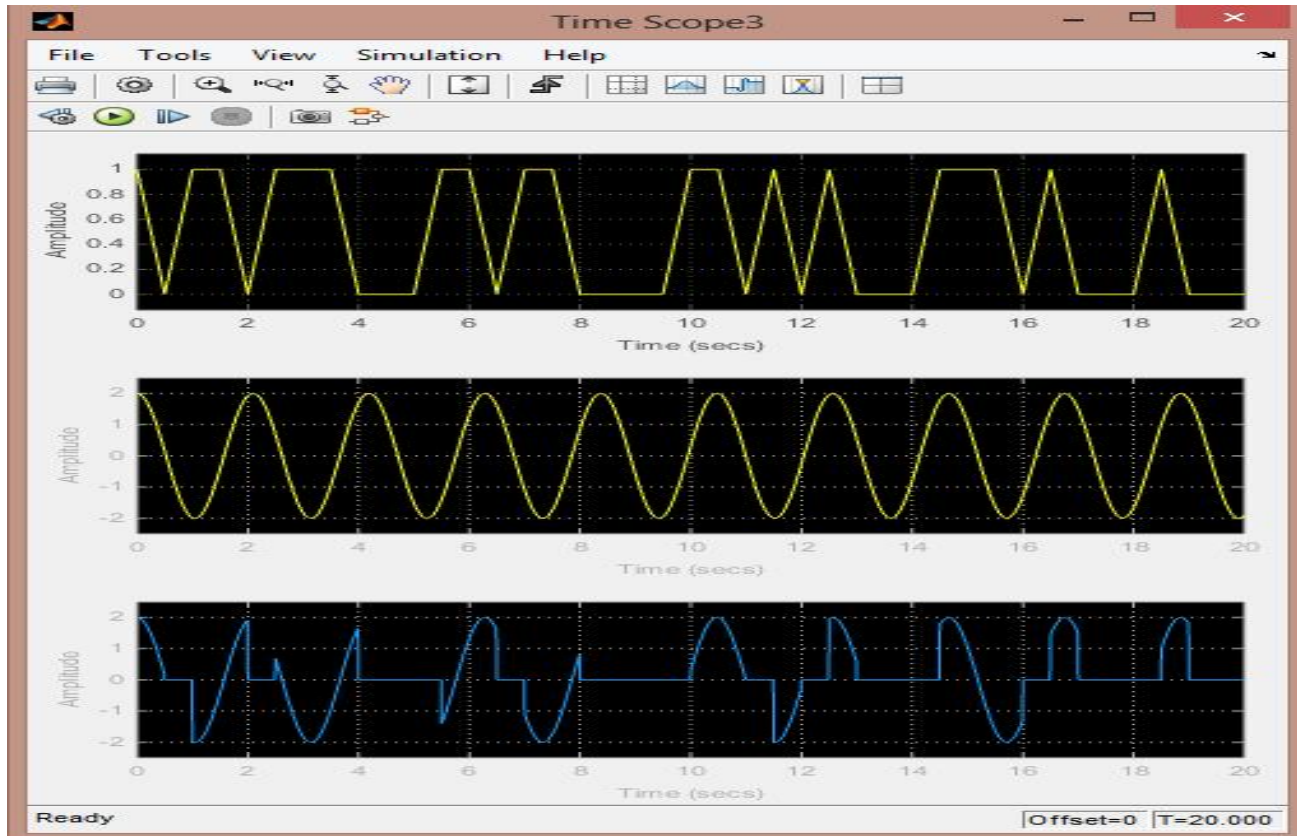
3. Carrier signal of 3 rads/sec

QPSK modulator signals

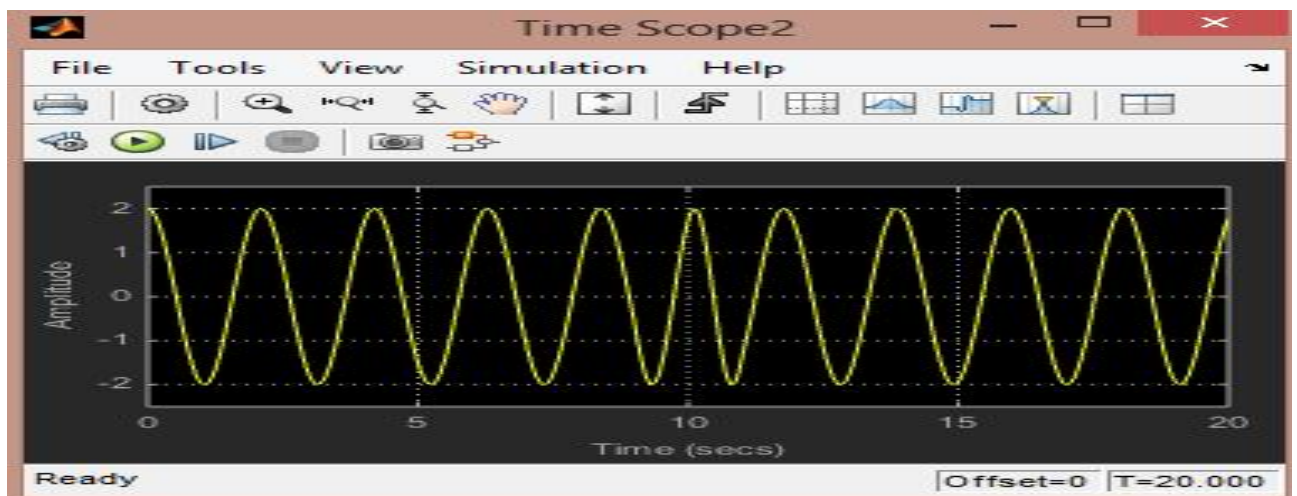
Top signal represents the message signal

Middle signal represents carrier signal used in QPSK modulation

Bottom signal represents QPSK modulated signal



Carrier signal recovered at 3 rads/sec



b) Discussion

The low pass used here is FIR (Finite Impulse Response). Most methods used to design this filter are based on ideal filter approximation. The large value of filter order was used since the transfer function of the FIR filter approaches the ideal as the filter order increases. The following are the reasons for the use of this filter; the filter can be exactly linear phase and the parameter of interest is phase, are always stable, and because there is no recursion, round off errors and overflow errors are easily controlled and may be realized by non-recursive structures which are simpler and more convenient for programming especially on devices specifically designed for digital signal processing. The main disadvantage is that large orders can be required to perform fairly simple filtering tasks. Complex to real and imaginary block was used to ensure that the signal that are driving the blocks is either real, imaginary or both. The limiter/saturation block was chosen instead of regenerators in the Q-arm and Inphase arm because regenerator amplifies the signal and noise but does not limit the amplitude of the noise. Limiter amplifies both the input signal and noise but limits the amplitude to a certain set value of the input so that at any one given time the noise amplitude does not exceed the required signal. The sampling time of the carrier signal must be the same as that of the voltage controlled oscillator for perfect carrier recovery. The sampling time used here falls between 0.01 to 0.1 seconds since high sampling time leads to some errors. The delay element is being reset from an external signal which is the signal from the summer. From the results obtained, the carrier recovered is the same as the carrier used in modulation. The slight variation in the carrier at 5rads/sec is brought about by the complex to real-imaginary block used to match the signals.

c) Analysis

1. Carrier signal at 10 rads/sec corresponds to 1.5915 Hz.

Carrier recovered: 20 seconds corresponds to 32cycles

$$1 \text{ second correspond to } \frac{1 \times 32}{20} = 1.6 \text{ cycles/ sec or } 1.6\text{Hz}$$

2. Carrier signal at 5 rads/sec corresponds to 0.7958 Hz

Carrier recovered: 20seconds corresponds to 16 cycles

$$1 \text{ second corresponds to } \frac{1 \times 16}{20} = 0.8 \text{ cycles/ sec or } 0.8\text{Hz}$$

3. Carrier signal at 3 rads/sec corresponds to 0.4775Hz

Carrier recovered: 20 seconds corresponds to 10 cycles

$$1 \text{ second correspond to } \frac{1 \times 10}{20} = 0.5\text{cycles/ sec or } 0.5\text{Hz}$$

CHAPTER 5

CONCLUSION AND RECOMMENDATIONS

a) Conclusion

The report talks about the design of carrier recovery by re-modulation circuit to be used in QPSK demodulation circuit. The circuit can operate in the frequency range of 88MHz to 108MHz that is the FM range.

The desired objectives were met but with the following conditions;

- (i) Sampling time of the carrier signal must be the same as that of voltage controlled oscillator.
- (ii) Sampling time must be between 0.01 and 0.1 seconds.
- (iii) Quiescent frequency of voltage control oscillator must be set to that of the carrier signal used for proper extraction of that carrier.
- (iv) Sampling frequency of the low pass filter must be two times higher than the highest frequency to avoid aliasing.
- (v) The delay element must be reset by an external signal coming from the summer to provide proper alignment between the QPSK modulated signal and the demodulated signal.
- (vi) The carrier signal used in QPSK modulation must be sinusoidal and the frequency must range from 0 rads/sec to 500 rads/sec.

From the above conditions and the analysis, the frequency of the carrier used is the same as that which has been recovered. Also the re-modulator side was able to do modulation as expected.

b) Recommendations

Although this design went a long way in designing a pure sine wave power buck, some of the set objectives were met(the carrier was recovered). I therefore recommend that a re-modulator loop which can be used in a multi-mission multiple data rate ground station be researched on and if possible be implemented in future. I also prefer that the circuit developed in Simulink be implemented in future. Finally I would recommend that a carrier recovery circuit that is able to extract a pulse type signal be investigated and simulated.

- REFERENCES**
- [1] John G. Proakis, Digital Communication 2nd edition, pages 303-318.
 - [2] John G. Proakis, Digital Communication 3rd edition, pages 333-350.
 - [3] Bernard E. Kerker, Eugen Strange, Digital Telephony and Network Integration 2nd edition, pages 167-177.
 - [4] Williams Stallings, Data and Computer Communications, pages 125-129.
 - [5] J.C. Bie D. Duponteil and J. C. Imbeaux, Elements of Digital Communications, pages 278-317.
 - [6] Bernard Sklar, Digital Communications Fundamentals and Applications 2nd edition, pages 167-200.
 - [7] Arthur B. Williams, Fred J. Taylor, Electronics Filter Design Handbook 3rd edition, chapter 3.
 - [8] William D. Stanley, Operational Amplifier With Linear Integrated Circuit 2nd edition, pages 217-221 and 500-501.
 - [9] Savant, Martin S Roden, Godon L. Carpenter, Electronics Design Circuits and Systems 2nd edition.
 - [10] Simon Hykin, Communication systems 4th edition.
 - [11] David R. Smith, Digital Transmission Systems 2nd edition, pages 353-391.
 - [12] www.isa.uma.es/c14/documentos/document_library/semin_simulink.pdf
 - [13] dali.field.cvut/ucebna/matlab/pdf_doc/comm./comm._tb.pdf
 - [14] Emmanuel C. Ifeachar, Digital Signal Processing a Practical Approach 2nd edition, pages 343-366.
 - [15] Ian A. Glover and Petter M Goat, Digital Communications 2nd edition, pages 391-408.

APPENDIX. Glossary

VCO.....Voltage Controlled Oscillator.

PSK.....Phase Shift Keying.

BPSK.....Binary Phase Shift Keying.

QPSK.....Quaternary Phase Shift Keying.

LPF.....Low Pass Filter.

PRK.....Phase Reversal Keying

IF.....Intermediate Frequency

LED.....Light Emitting Diode

FET.....Field Effect Transistor

BJT.....Bipolar Junction Transistor

OP-AMPS..Operational Amplifier